

General Description

The series of devices use advanced trench gate super junction technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. This super junction MOSFET fits the industry's AC-DC SMPS requirements for PFC, AC/DC power conversion, and industrial power applications.

Features

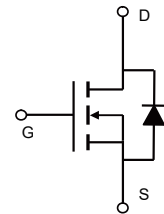
- New technology for high voltage device
- Low on-resistance and low conduction losses
- Small package
- Ultra Low Gate Charge cause lower driving requirements
- 100% Avalanche Tested
- ROHS compliant

Application

- Power factor correction (PFC)
- Switched mode power supplies(SMPS)
- Uninterruptible Power Supply (UPS)



1 2 3
TO-220



Schematic

Parameter	Symbol	Q1	Q2	Unit
Drain-Source Voltage ($V_{GS}=0V$)	V_{DS}	700		V
Gate-Source Voltage ($V_{DS}=0V$) AC ($f>1$ Hz)	V_{GS}	± 30		V
Continuous Drain Current at $T_c=25^\circ C$	$I_{D(DC)}$	15	15*	A
Continuous Drain Current at $T_c=100^\circ C$	$I_{D(DC)}$	10	10*	A
Pulsed drain current (Note 1)	$I_{DM(pluse)}$	60	60*	A
Maximum Power Dissipation($T_c=25^\circ C$)	P_D	131	33.2	W
Derate above $25^\circ C$		1.05	0.265	W/ $^\circ C$
Single pulse avalanche energy (Note 2)	EAS	304		mJ
Avalanche current(Note 1)	I_{AR}	3		A
Repetitive Avalanche energy , t_{AR} limited by T_{jmax} (Note 1)	E_{AR}	1.6		mJ

Parameter	Symbol	Q1	Q2	Unit
Drain Source voltage slope, $V_{DS} \leq 480V$,	dv/dt	50		V/ns
Reverse diode dv/dt , $V_{DS} \leq 480V, I_{SD} < I_D$	dv/dt	15		V/ns
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55...+150		°C

* limited by maximum junction temperature

Table 2. Thermal Characteristic

Parameter	Symbol	Q1	Q2	Unit
Thermal Resistance, Junction-to-Case (Maximum)	R_{thJC}	0.95	3.76	°C / W
Thermal Resistance, Junction-to-Ambient (Maximum)	R_{thJA}	62	80	°C / W

Table 3. Electrical Characteristics (TA=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
On/off states						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA	700			V
Zero Gate Voltage Drain Current(Tc=25℃)	I _{DSS}	V _{DS} =700V, V _{GS} =0V			1	μA
Zero Gate Voltage Drain Current(Tc=125℃)	I _{DSS}	V _{DS} =700V, V _{GS} =0V			100	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V			±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	3	3.5	4	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =8A		260	290	mΩ
Dynamic Characteristics						
Input Capacitance	C _{iss}	V _{DS} =50V, V _{GS} =0V, F=1.0MHz		1210	1400	pF
Output Capacitance	C _{oss}			74		pF
Reverse Transfer Capacitance	C _{rss}			0.2		pF
Total Gate Charge	Q _g	V _{DS} =480V, I _D =15A, V _{GS} =10V		24.7	42	nC
Gate-Source Charge	Q _{gs}			8.2		nC
Gate-Drain Charge	Q _{gd}			8.5		nC
Switching times						
Turn-on Delay Time	t _{d(on)}	V _{DD} =420V, I _D =8A, R _G =2.3Ω, V _{GS} =10V		15		nS
Turn-on Rise Time	t _r			10		nS
Turn-Off Delay Time	t _{d(off)}			57		nS
Turn-Off Fall Time	t _f			9		nS
Source- Drain Diode Characteristics						
Source-drain current(Body Diode)	I _{SD}	T _c =25℃			15	A
Pulsed Source-drain current(Body Diode)	I _{SDM}				60	A
Forward On Voltage	V _{SD}	T _j =25℃, I _{SD} =15A, V _{GS} =0V		0.9	1.2	V
Reverse Recovery Time	t _{rr}	T _j =25℃, I _F =7.5A, di/dt=100A/μs		240		nS
Reverse Recovery Charge	Q _{rr}			2		uC
Peak Reverse Recovery Current	I _{rrm}			17		A

Notes 1.Repetitive Rating: Pulse width limited by maximum junction temperature

2. $T_J=25^\circ C, V_{DD}=50V, V_G=10V, R_G=25\Omega$

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS (curves)

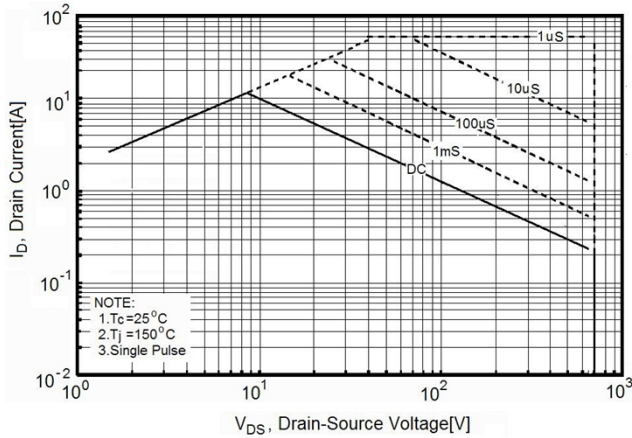
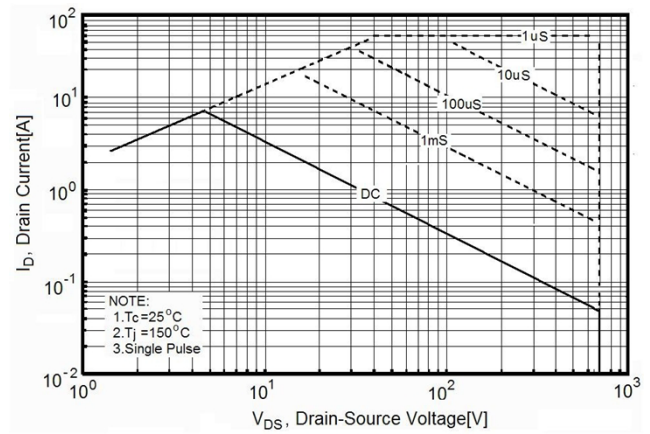
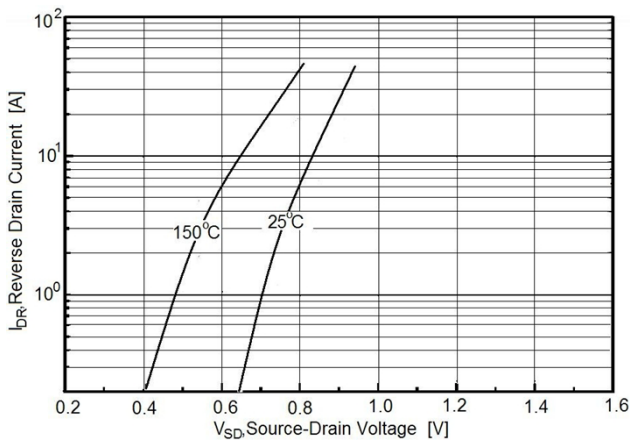
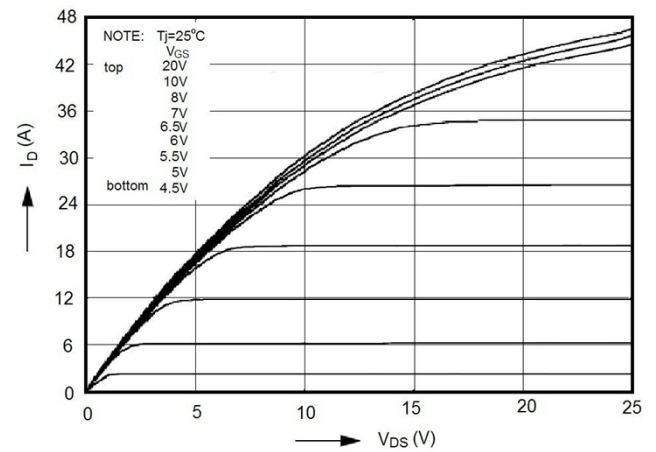
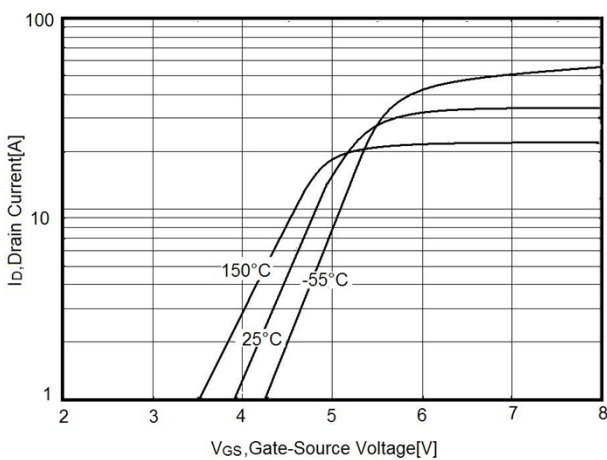
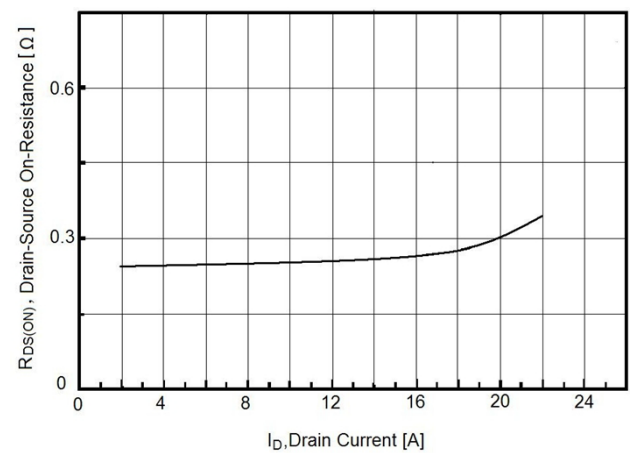
Figure1. Safe operating area

Figure2. Safe operating area for TO-220F

Figure3. Source-Drain Diode Forward Voltage

Figure4. Output characteristics

Figure5. Transfer characteristics

Figure6. Static drain-source on resistance


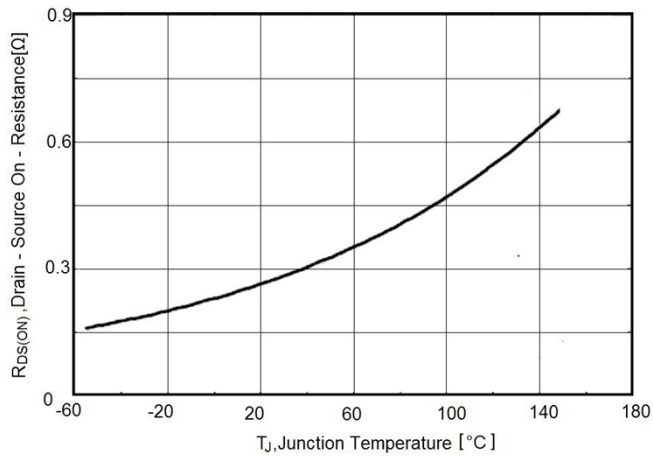
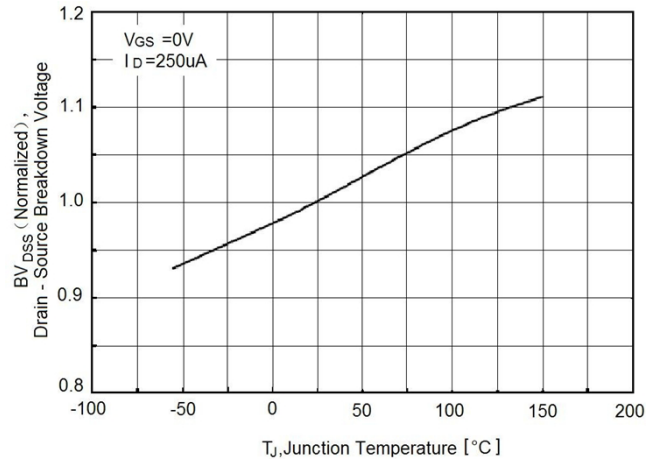
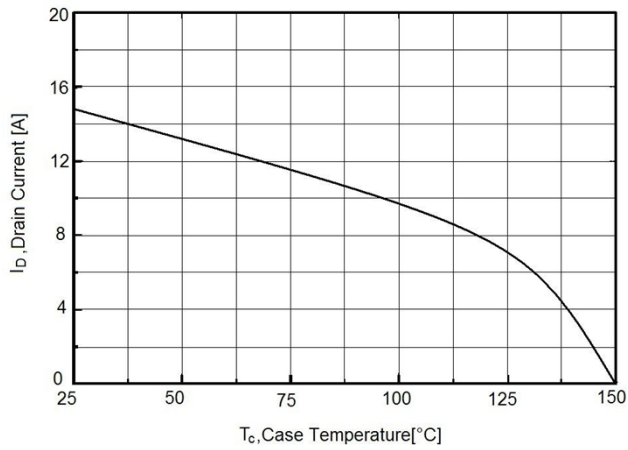
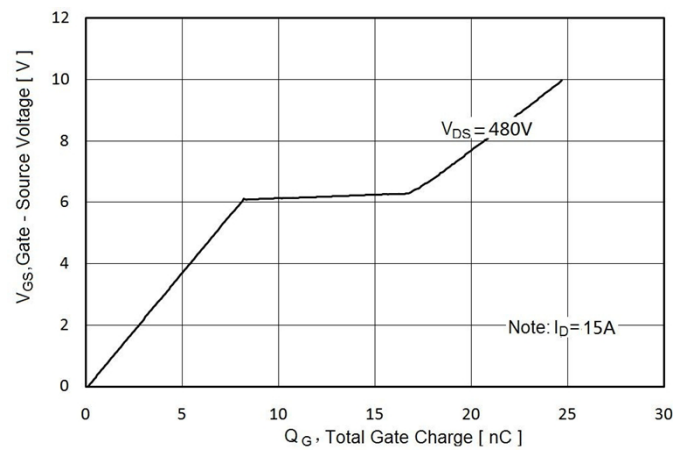
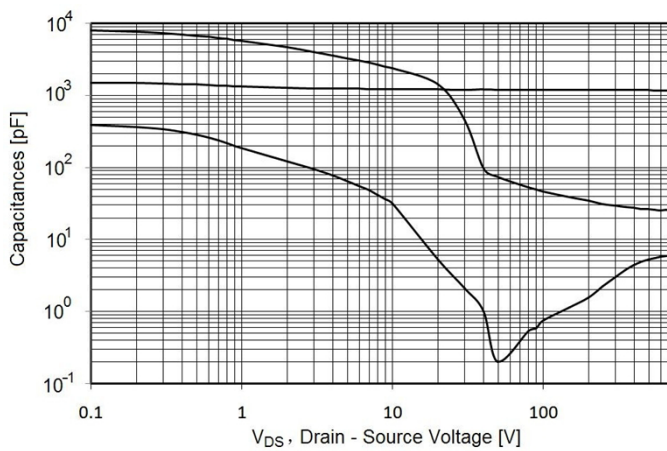
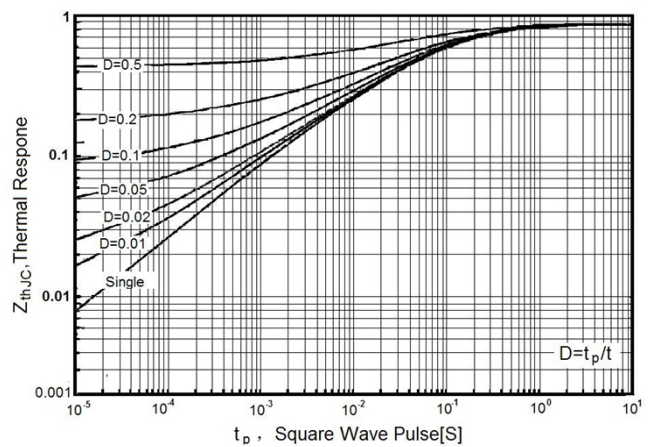
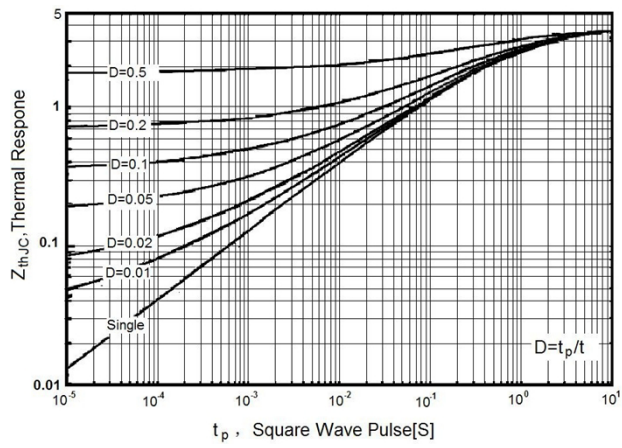
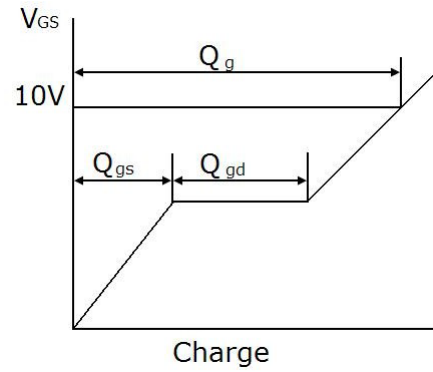
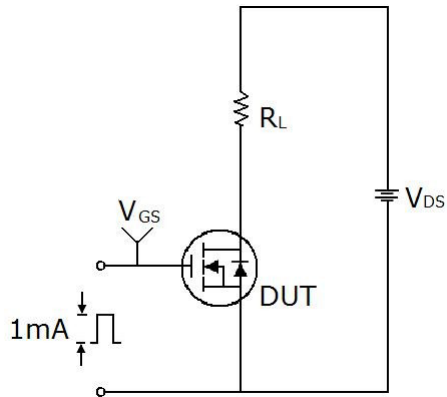
Figure7. $R_{DS(ON)}$ vs Junction Temperature

Figure8. BV_{DSS} vs Junction Temperature

Figure9. Maximum I_D vs Junction Temperature

Figure10. Gate charge waveforms

Figure11. Capacitance

Figure12. Transient Thermal Impedance


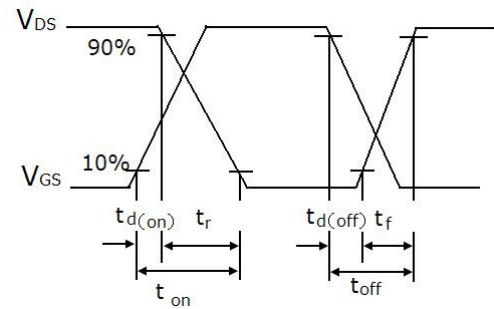
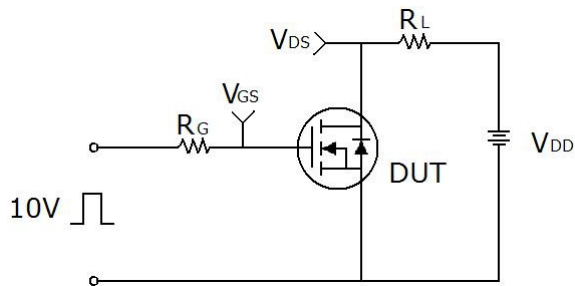
Figure13. Transient Thermal Impedance for TO-220F

Test circuit

1) Gate charge test circuit & Waveform



2) Switch Time Test Circuit:



3) Unclamped Inductive Switching Test Circuit & Waveforms

