

General Description

The series of devices use advanced trench gate super junction technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. This super junction MOSFET fits the industry's AC-DC SMPS requirements for PFC, AC/DC power conversion, and industrial power applications.

Features

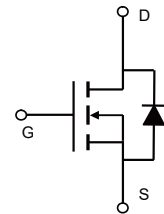
- New technology for high voltage device
- Low on-resistance and low conduction losses
- small package
- Ultra Low Gate Charge cause lower driving requirements
- 100% Avalanche Tested
- ROHS compliant

Application

- Power factor correction (PFC)
- Switched mode power supplies(SMPS)



TO-220



Schematic

Parameter	Symbol	Q1	Q2	Unit
Drain-Source Voltage ($V_{GS}=0V$)	V_{DS}	700		V
Gate-Source Voltage ($V_{DS}=0V$), AC($f>1Hz$)	V_{GS}	± 30		V
Continuous Drain Current at $T_C=25^\circ C$	$I_{D(DC)}$	11.5	11.5*	A
Continuous Drain Current at $T_C=100^\circ C$	$I_{D(DC)}$	7	7*	A
Pulsed drain current (Note 1)	$I_{DM(pluse)}$	46	46*	A
Maximum Power Dissipation($T_C=25^\circ C$) Derate above $25^\circ C$	P_D	101 0.81	32.6 0.26	W W/ $^\circ C$
Single pulse avalanche energy (Note2)	EAS	144		mJ
Avalanche current(Note 2)	IAS	3		A
Repetitive Avalanche energy , t_{AR} limited by T_{jmax} (Note 1)	E_{AR}	0.5		mJ

Parameter	Symbol	Q1	Q2	Unit
Drain Source voltage slope, $V_{DS} \leq 480V$,	dv/dt	50		V/ns
Reverse diode dv/dt , $V_{DS} \leq 480V, I_{SD} < I_D$	dv/dt	15		V/ns
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55...+150		°C

* limited by maximum junction temperature

Table 2. Thermal Characteristic

Parameter	Symbol	Q1	Q2	Unit
Thermal Resistance, Junction-to-Case (Maximum)	R_{thJC}	1.24	3.83	°C / W
Thermal Resistance, Junction-to-Ambient (Maximum)	R_{thJA}	62	80	°C / W

Table 3. Electrical Characteristics (TA=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
On/off states						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	700			V
Zero Gate Voltage Drain Current($T_c=25^{\circ}C$)	I_{DSS}	$V_{DS}=700V, V_{GS}=0V$		0.05	1	μA
Zero Gate Voltage Drain Current($T_c=125^{\circ}C$)	I_{DSS}	$V_{DS}=700V, V_{GS}=0V$			100	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$			± 100	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	3	3.5	4	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=7A$		360	420	m Ω
Dynamic Characteristics						
Input Capacitance	C_{iss}	$V_{DS}=50V, V_{GS}=0V,$ $F=1.0MHz$		870		pF
Output Capacitance	C_{oss}			54		pF
Reverse Transfer Capacitance	C_{rss}			1.8		pF
Total Gate Charge	Q_g	$V_{DS}=480V, I_D=11.5A,$ $V_{GS}=10V$		19		nC
Gate-Source Charge	Q_{gs}			6		nC
Gate-Drain Charge	Q_{gd}			6.5		nC
Switching times						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=420V, I_D=5.5A,$ $R_G=3\Omega, V_{GS}=10V$		12		nS
Turn-on Rise Time	t_r			9		nS
Turn-Off Delay Time	$t_{d(off)}$			61	70	nS
Turn-Off Fall Time	t_f			11	14	nS
Source- Drain Diode Characteristics						
Source-drain current(Body Diode)	I_{SD}	$T_c=25^{\circ}C$			11.5	A
Pulsed Source-drain current(Body Diode)	I_{SDM}				46	A
Forward on voltage	V_{SD}	$T_j=25^{\circ}C, I_{SD}=11.5A, V_{GS}=0V$		0.9	1.2	V
Reverse Recovery Time	t_{rr}	$T_j=25^{\circ}C, I_F=5.8A,$ $di/dt=100A/\mu s$		220		nS
Reverse Recovery Charge	Q_{rr}			2.2		μC
Peak Reverse Recovery Current	I_{rrm}			19		A

Notes: 1.Repetitive Rating: Pulse width limited by maximum junction temperature

2. $T_J=25^\circ C, V_{DD}=50V, V_G=10V, R_G=25\Omega$

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS (curves)

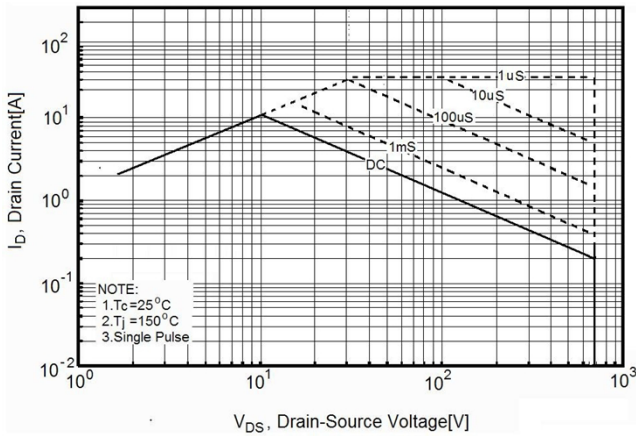
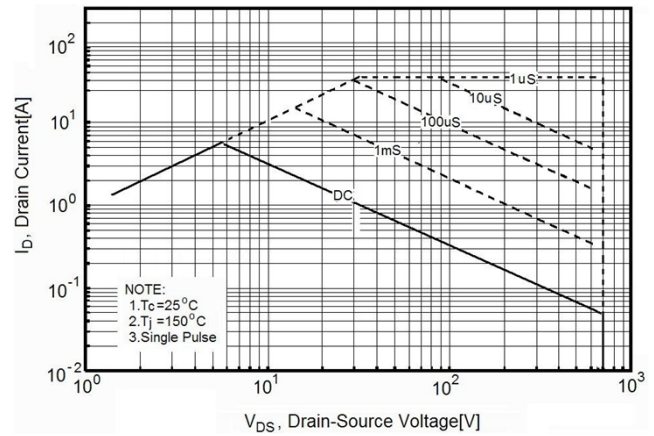
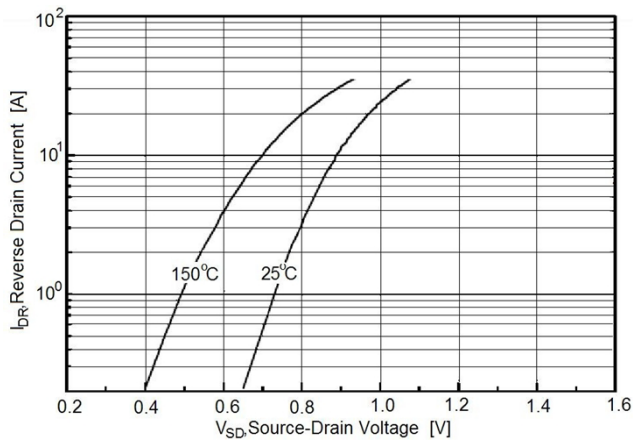
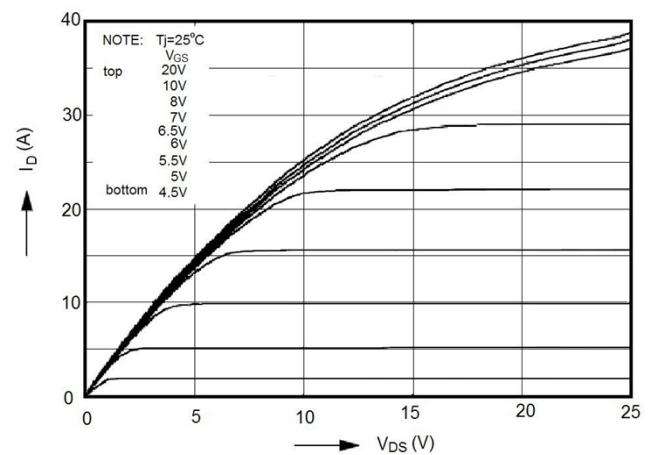
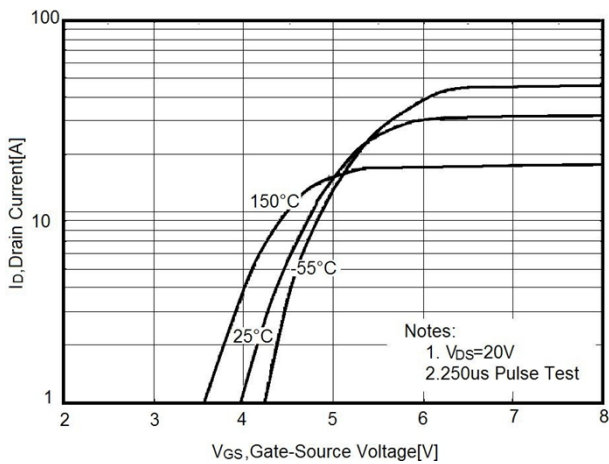
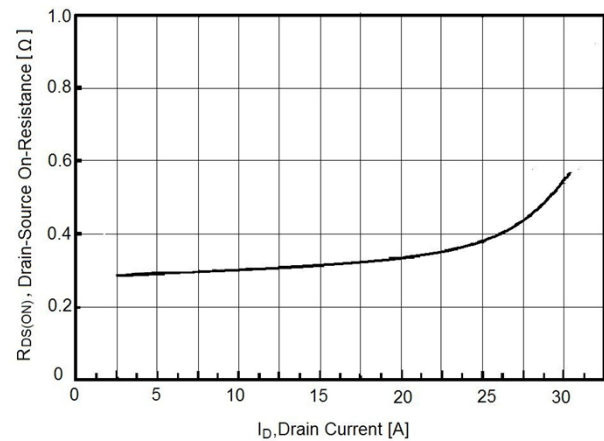
Figure1. Safe operating area

Figure2. Safe operating area for TO-220F

Figure3. Source-Drain Diode Forward Voltage

Figure4. Output characteristics

Figure5. Transfer characteristics

Figure6. Static drain-source on resistance


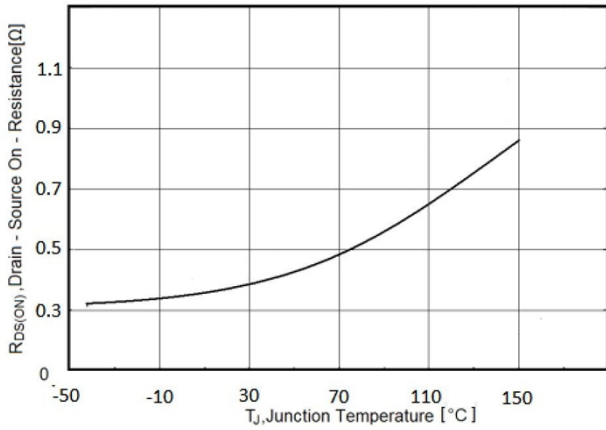
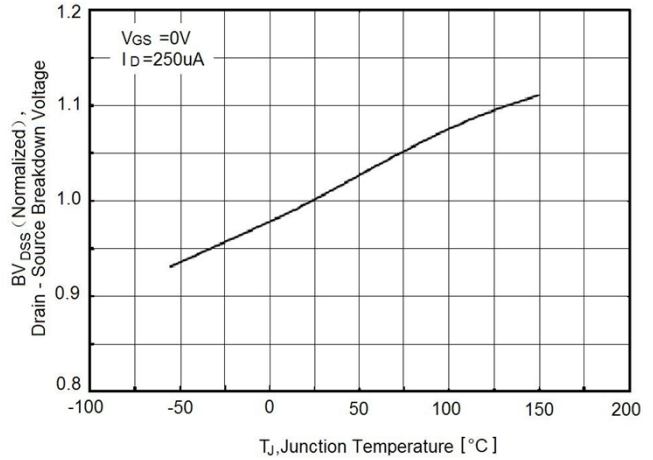
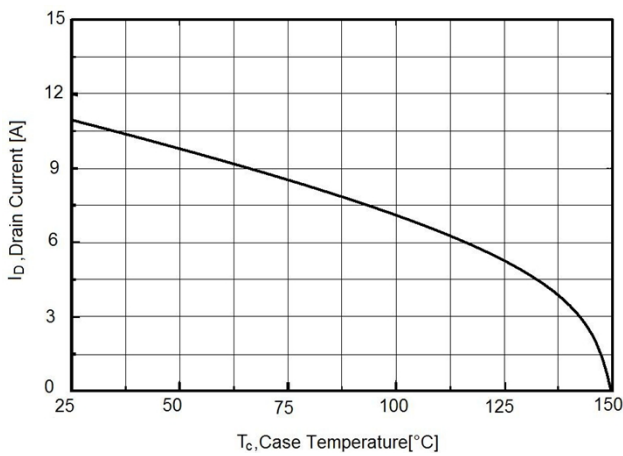
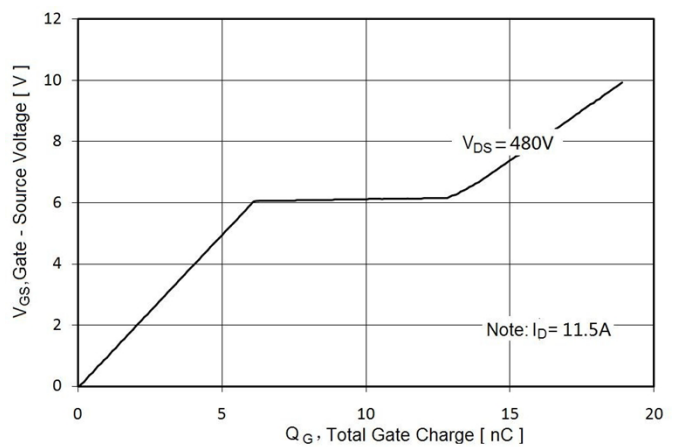
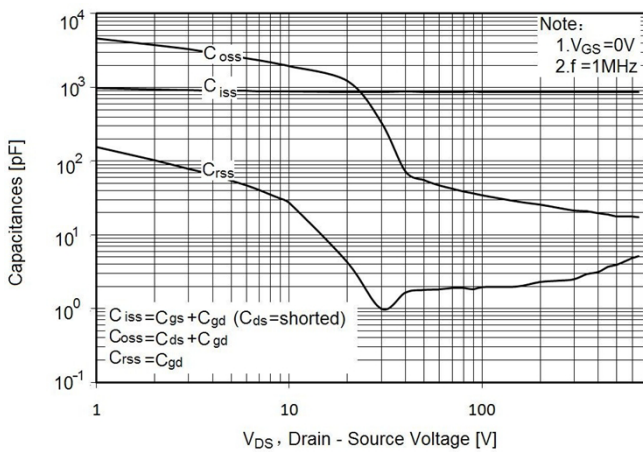
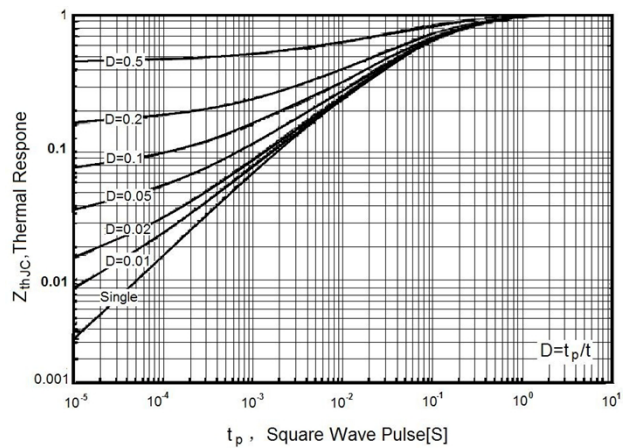
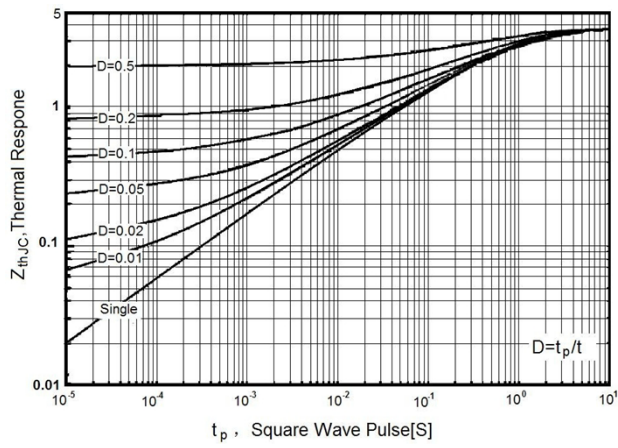
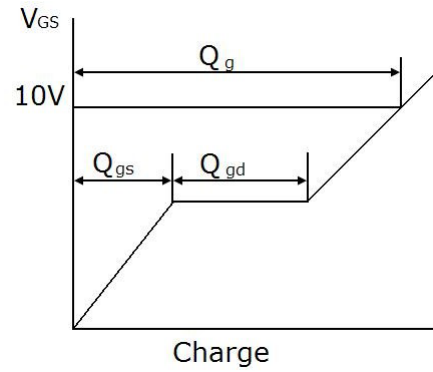
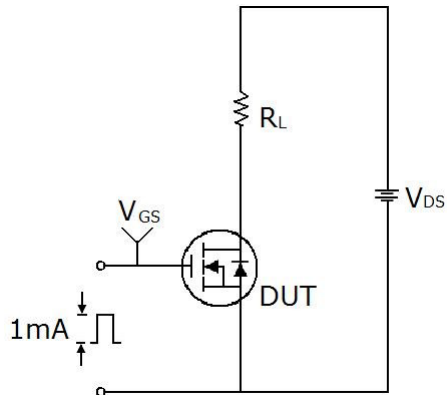
Figure7. $R_{DS(ON)}$ vs Junction Temperature

Figure8. BV_{DSS} vs Junction Temperature

Figure9. Maximum I_D vs Junction Temperature

Figure10. Gate charge waveforms

Figure11. Capacitance

Figure12. Transient Thermal Impedance


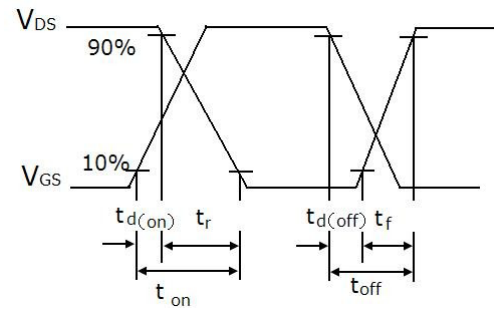
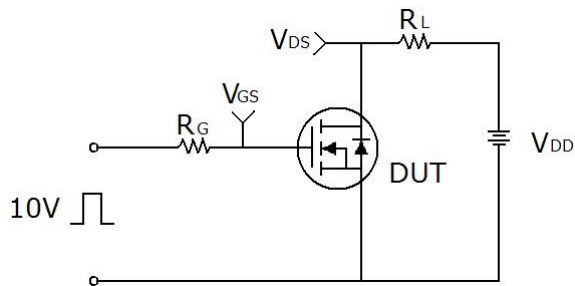
Figure13. Transient Thermal Impedance for TO-220F

Test circuit

1) Gate charge test circuit & Waveform



2) Switch Time Test Circuit:



3) Unclamped Inductive Switching Test Circuit & Waveforms

