Description

The VSM5NP06 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

General Features

N channel

- V_{DS} =60V,I_D =5A
  $R_{DS(ON)}$ <28mΩ @ V_{GS}=10V
  $R_{DS(ON)}$ <38mΩ @ V_{GS}=4.5V

P channel

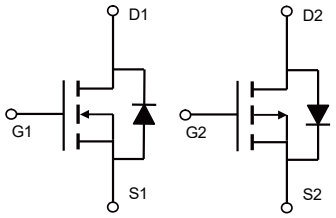
- V_{DS} =-60V,I_D =-4A
  $R_{DS(ON)}$ <80mΩ @ V_{GS}=-10V

- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- 100% Rg tested
- 100% ΔVds tested
- 100% UIS tested

Application

- H-bridge
- Inverters

SOP-8



Schematic

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
VSM5NP06	VSM5NP06-S8	SOP-8	Ø330mm	12mm	4000 units

Absolute Maximum Ratings (T_A=25℃unless otherwise noted)

Parameter		Symbol	N-Channel	P-Channel	Unit
Drain-Source Voltage		V_{DS}	60	-60	V
Gate-Source Voltage		V_{GS}	±20	±20	V
Continuous Drain Current	T_A=25℃	I_D	5	-4	A
	T_A=100℃		3.5	-2.8	
Pulsed Drain Current (Note 1)		I_{DM}	30	-30	A
Maximum Power Dissipation	T_A=25℃	P_D	2	2	W
Operating Junction and Storage Temperature Range		T_J,T_{STG}	-55 To 150	-55 To 150	℃

Thermal Characteristic

N-channel	Thermal Resistance,Junction-to- Ambient (Note 2)	$R_{\theta JA}$	62.5	℃/W
P-channel	Thermal Resistance,Junction-to- Ambient (Note 2)	$R_{\theta JA}$	62.5	℃/W
N-channel	Thermal Resistance,Junction-to- Lead (Note 2)	$R_{\theta JL}$	30	℃/W
P-channel	Thermal Resistance,Junction-to- Lead (Note 2)	$R_{\theta JL}$	30	℃/W

N-Channel Electrical Characteristics (T_A=25℃unless otherwise noted)

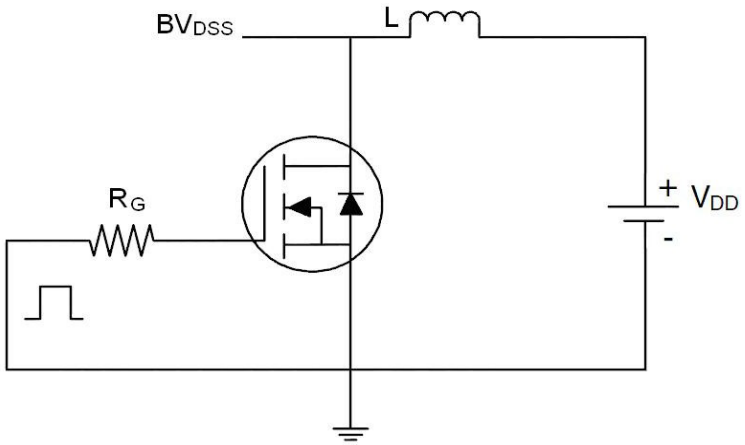
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=250μA	60	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=60V,V_{GS}=0V	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA	1.0	1.6	2.5	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=5A	-	24	28	mΩ
	$R_{DS(ON)}$	V_{GS}=4.5V, I_D=5A		32	38	mΩ
Forward Transconductance	g_{FS}	V_{DS}=5V,I_D=5A	11	-	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C_{lss}	V_{DS}=30V,V_{GS}=0V, F=1.0MHz	-	979	-	PF
Output Capacitance	C_{oss}		-	120	-	PF
Reverse Transfer Capacitance	C_{rss}		-	100	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=30V ,R_L=2.5Ω V_{GS}=10V,R_G=3Ω	-	4.2	-	nS
Turn-on Rise Time	t_r		-	3.4	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	16	-	nS
Turn-Off Fall Time	t_f		-	2	-	nS
Total Gate Charge	Q_g	V_{DS}=30V,I_D=5A, V_{GS}=10V	-	22		nC
Gate-Source Charge	Q_{gs}		-	3.3		nC
Gate-Drain Charge	Q_{gd}		-	5.2		nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	V_{GS}=0V,I_S=5A	-		1.2	V
Diode Forward Current (Note 2)	I_S		-	-	5	A
Reverse Recovery Time	t_{rr}	TJ = 25°C, IF =5A di/dt = 100A/μs(Note3)	-	27	-	nS
Reverse Recovery Charge	Qrr		-	30	-	nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

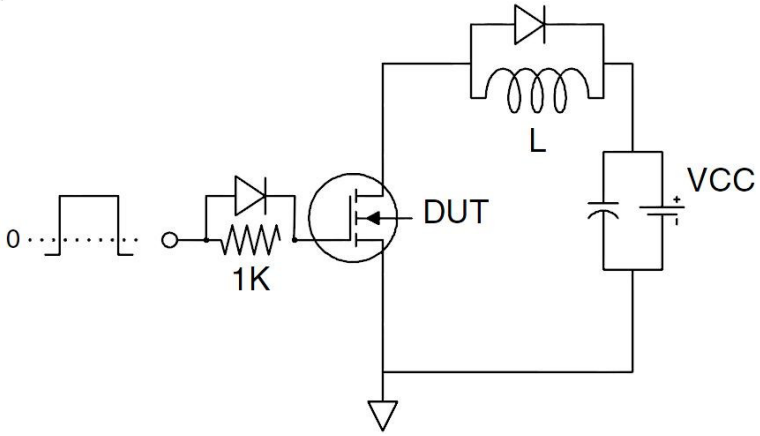
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with TA =25°C. The value in any a given application depends on the user's specific board design. The $R_{\theta JA}$ i is the sum of the thermal impedence from junction to lead $R_{\theta JL}$ and lead to ambient..
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production

Test Circuit

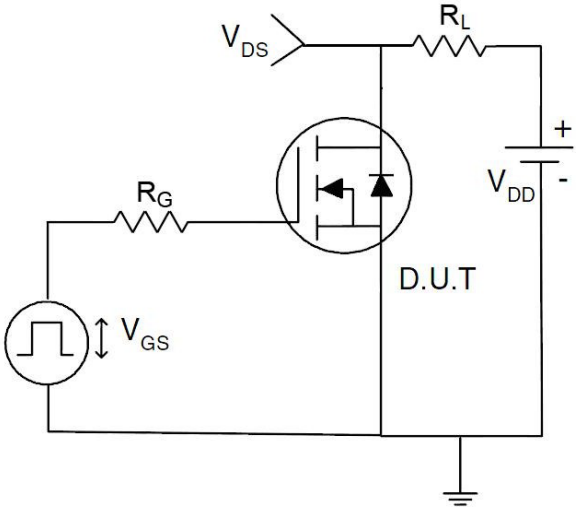
1) E_{AS} test Circuit



2) Gate charge test Circuit



3) Switch Time Test Circuit



N-Channel Typical Electrical and Thermal Characteristics (Curves)

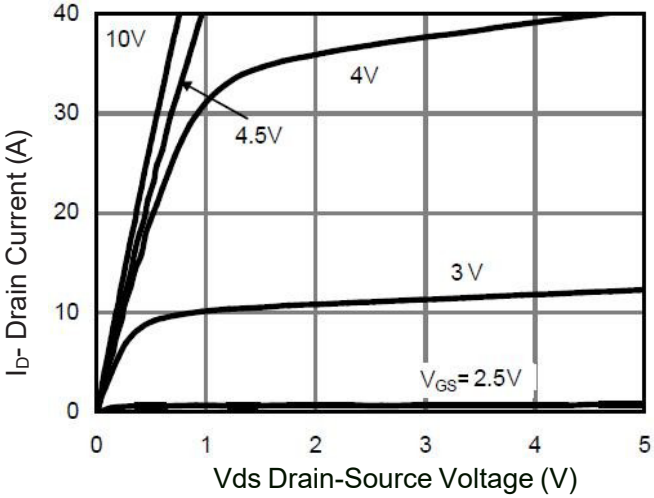


Figure 1 Output Characteristics

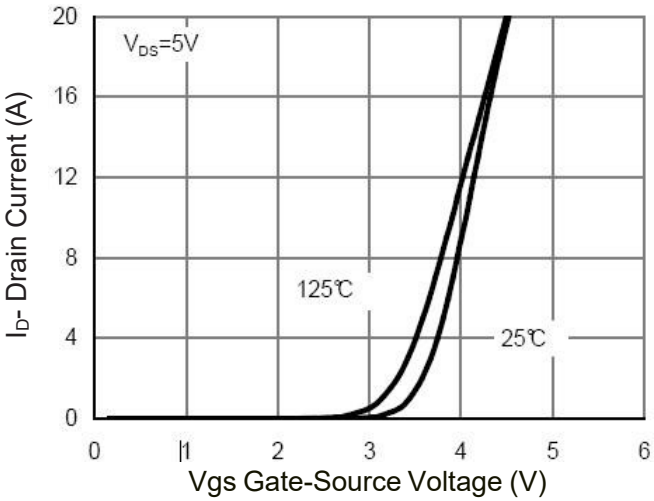


Figure 2 Transfer Characteristics

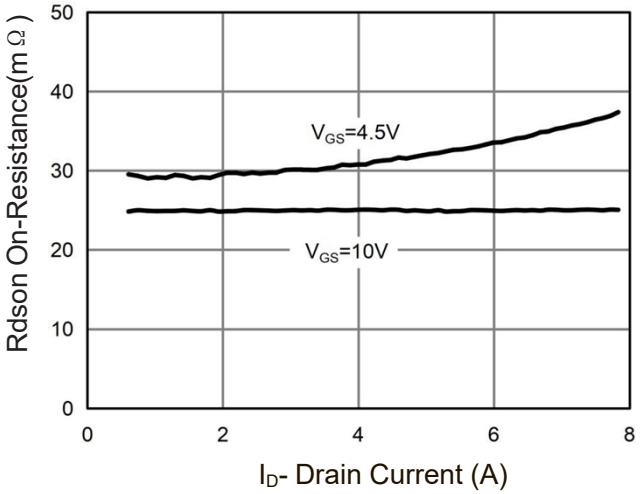


Figure 3 Rdson- Drain Current

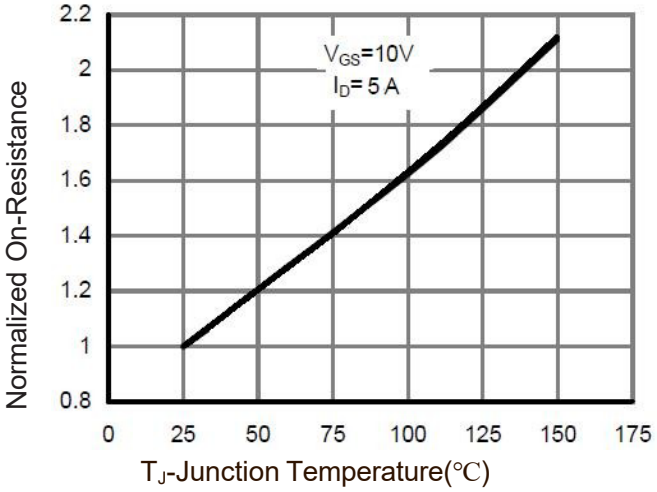


Figure 4 Rdson-Junction Temperature

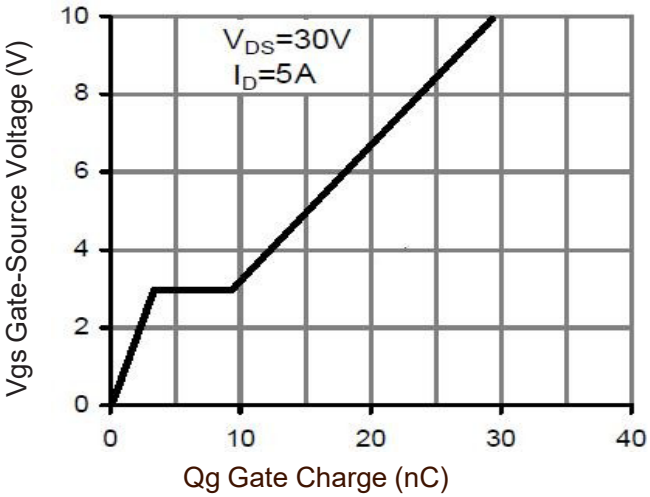


Figure 5 Gate Charge

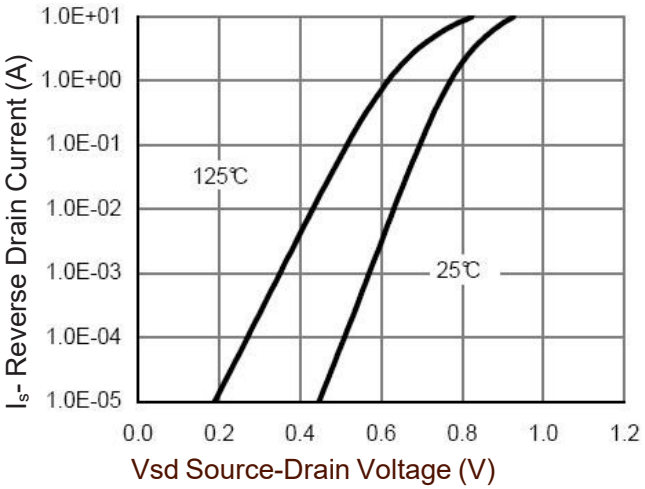


Figure 6 Source- Drain Diode Forward

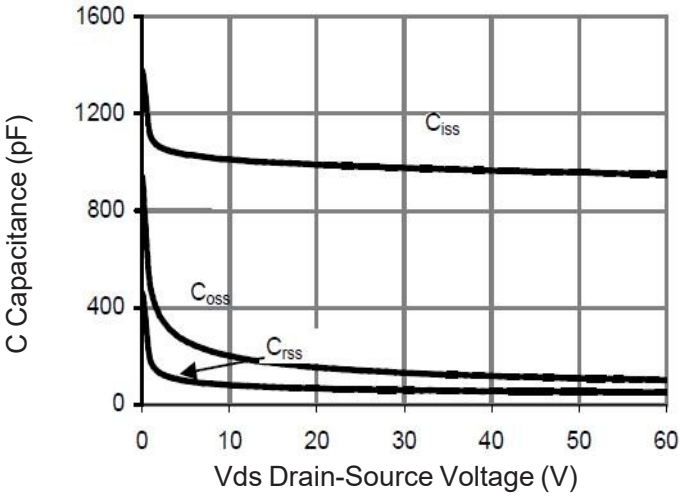


Figure 7 Capacitance vs Vds

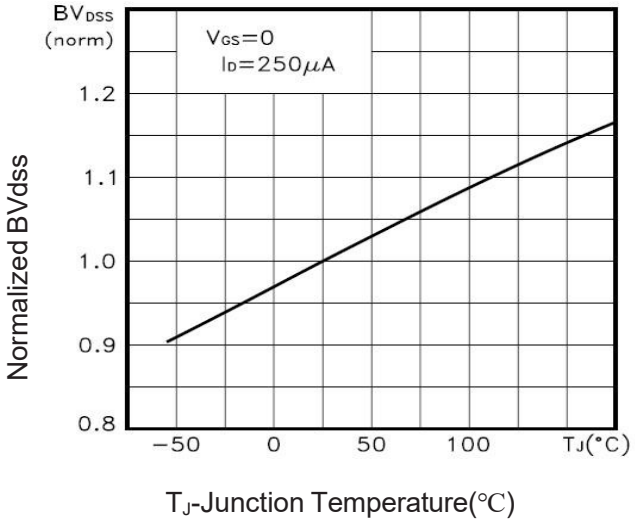


Figure 9 BV_{DSS} vs Junction Temperature

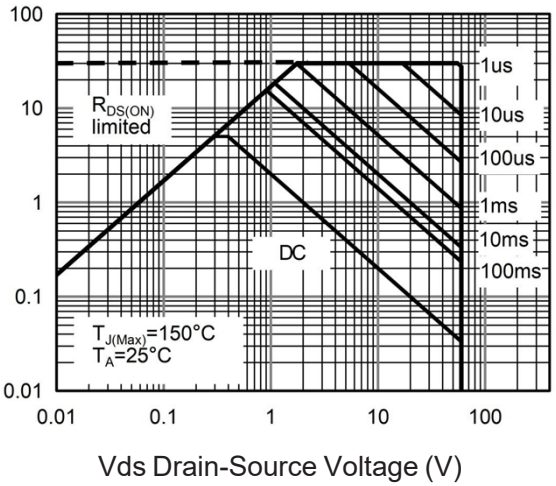


Figure 8 Safe Operation Area

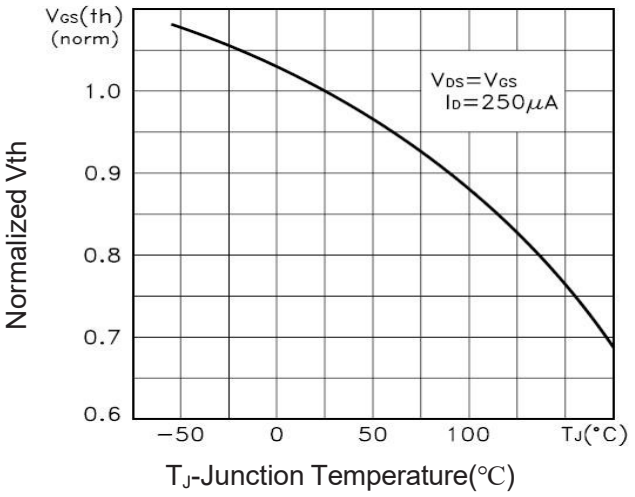


Figure 10 $V_{GS(th)}$ vs Junction Temperature

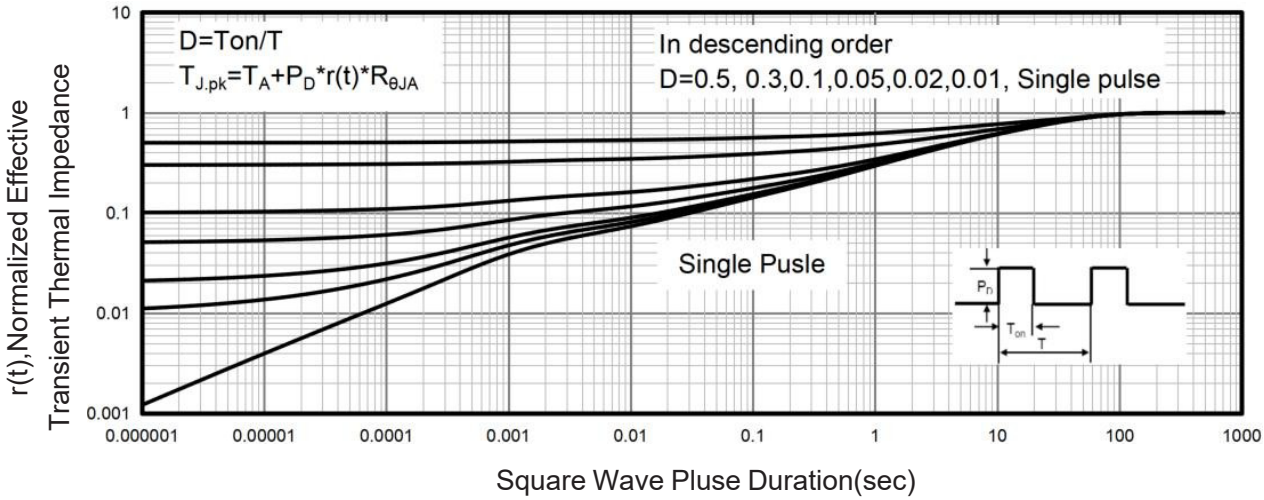


Figure 11 Normalized Maximum Transient Thermal Impedance

P-Channel Electrical Characteristics (T_A=25℃unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=-250μA	-60	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-60V,V_{GS}=0V	-	-	-1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=-250μA	-1.5	-2.6	-3.0	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=-10V, I_D=-4A	-	64	80	mΩ
Forward Transconductance	g_{FS}	V_{DS}=-5V,I_D=-4A	11	-	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C_{lss}	V_{DS}=-30V,V_{GS}=0V, F=1.0MHz	-	960	-	PF
Output Capacitance	C_{oss}		-	86	-	PF
Reverse Transfer Capacitance	C_{rss}		-	38	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=-30V ,R_L=2.5Ω V_{GS}=-10V,R_G=3Ω	-	9	-	nS
Turn-on Rise Time	t_r		-	10	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	25	-	nS
Turn-Off Fall Time	t_f		-	11	-	nS
Total Gate Charge	Q_g	V_{DS}=-30V,I_D=-4A, V_{GS}=10V	-	15.8		nC
Gate-Source Charge	Q_{gs}		-	3		nC
Gate-Drain Charge	Q_{gd}		-	3.5		nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	V_{GS}=0V,I_S=-4A	-		-1.2	V
Diode Forward Current (Note 2)	I_S		-	-	-4	A
Reverse Recovery Time	t_{rr}	TJ = 25°C, IF =-4A di/dt = 100A/μs(Note3)	-	27.5	-	nS
Reverse Recovery Charge	Qrr		-	30	-	nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.

2. The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with TA =25°C. The value in any a given application depends on the user's specific board design. The $R_{\theta JA}$ i is the sum of the thermal impedence from junction to lead $R_{\theta JL}$ and lead to ambient..

3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.

4. Guaranteed by design, not subject to production

P-Channel Typical Electrical and Thermal Characteristics (Curves)

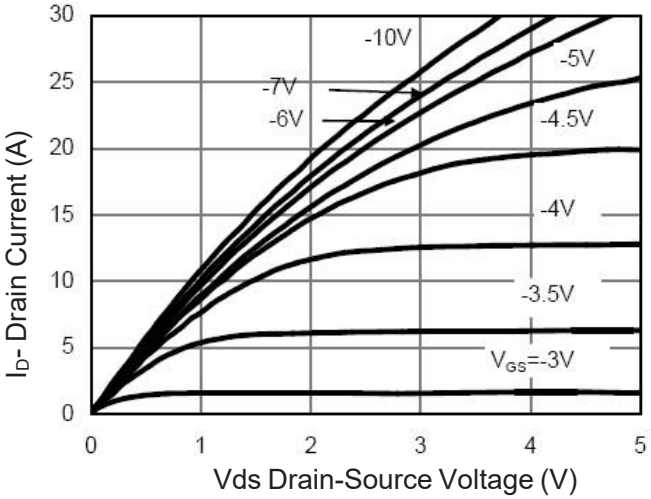


Figure 1 Output Characteristics

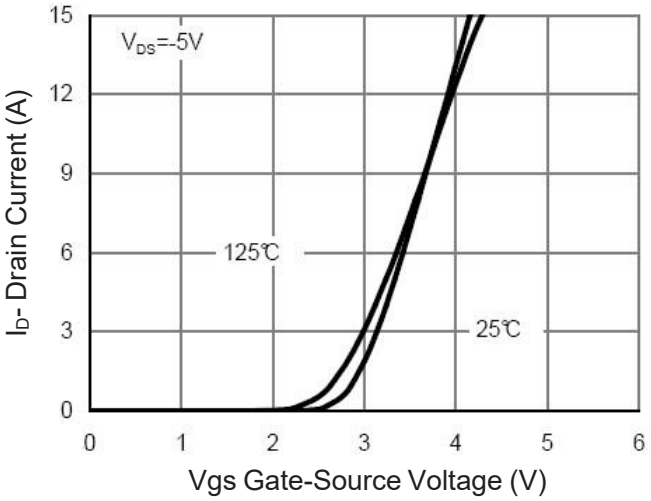


Figure 2 Transfer Characteristics

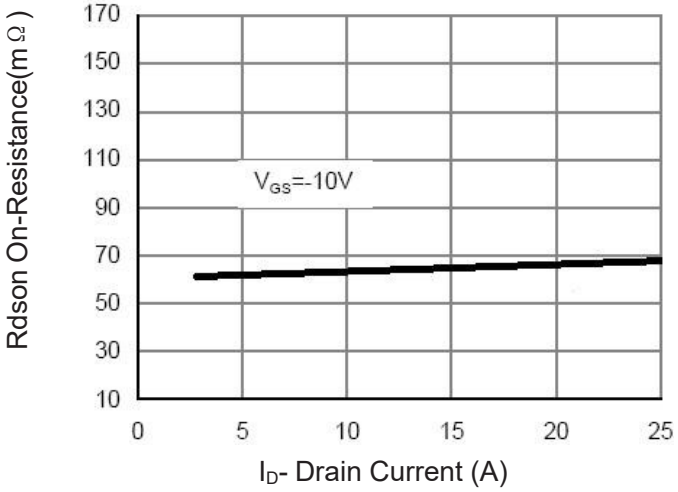


Figure 3 Rdson- Drain Current

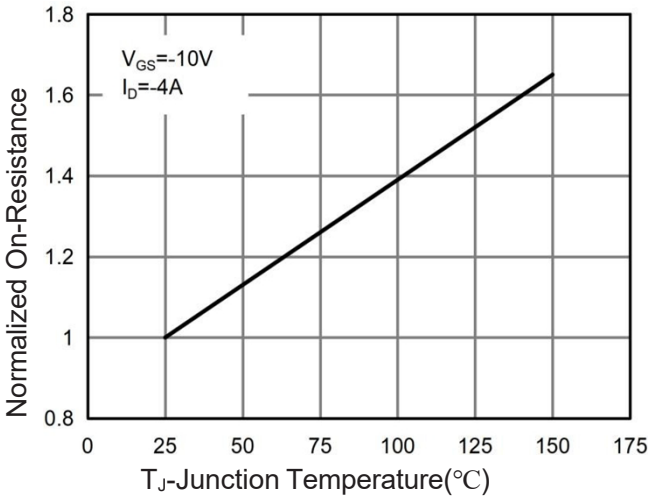


Figure 4 Rdson-Junction Temperature

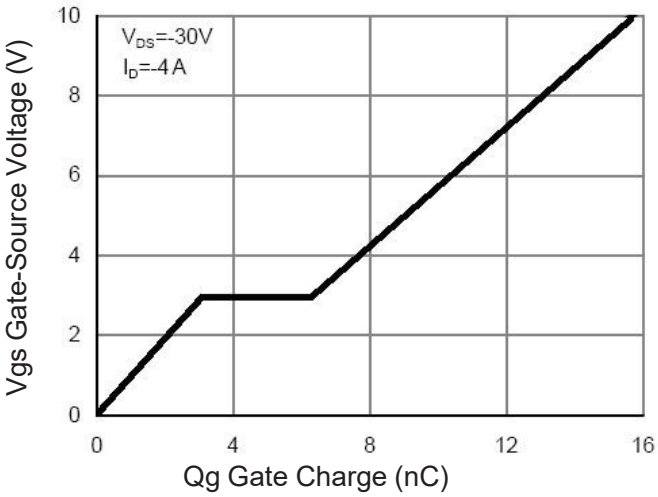


Figure 5 Gate Charge

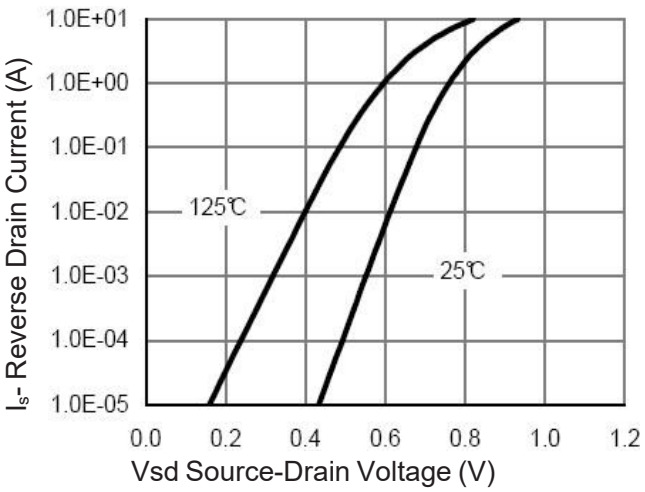


Figure 6 Source- Drain Diode Forward

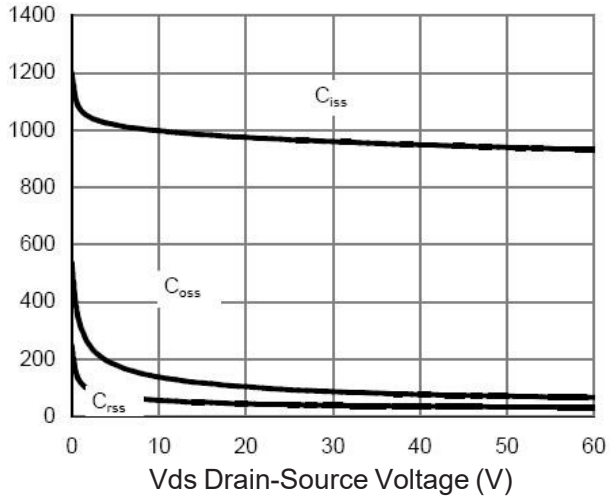


Figure 7 Capacitance vs Vds

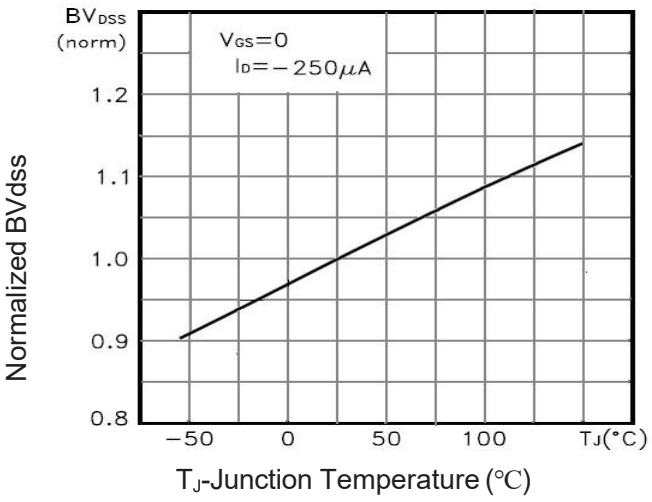


Figure 9 BV_{DSS} vs Junction Temperature

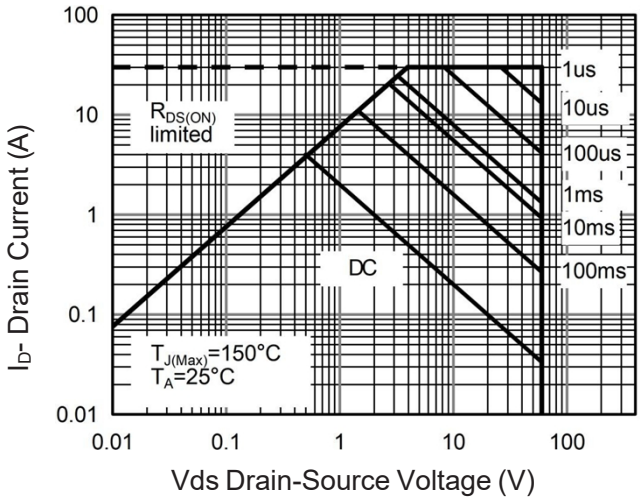


Figure 8 Safe Operation Area

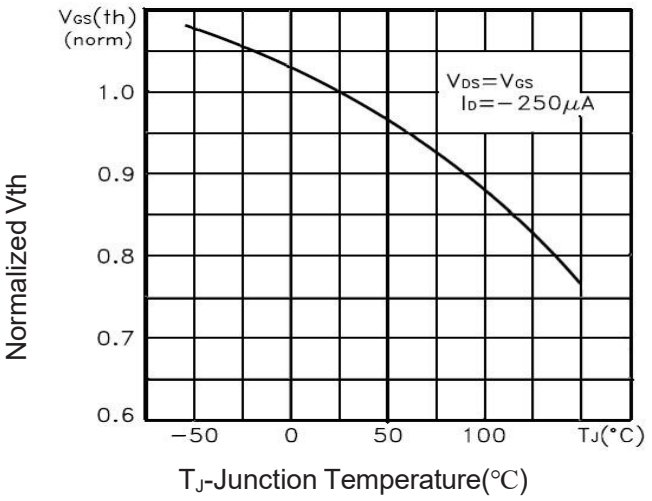


Figure 10 $V_{GS(th)}$ vs Junction Temperature

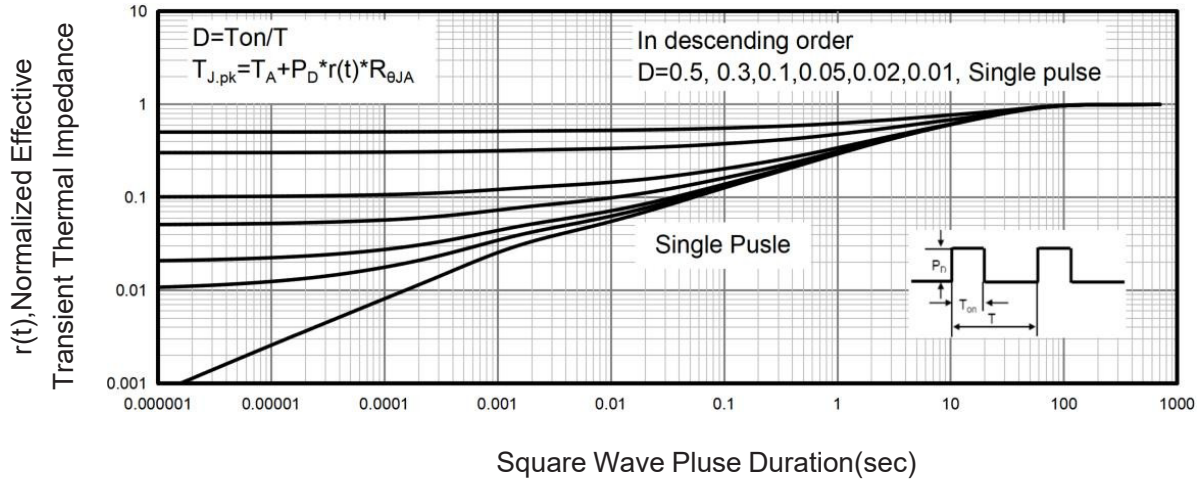


Figure 11 Normalized Maximum Transient Thermal Impedance