Description

The VSM6NP04 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$,low gate charge. It can be used in a wide variety of applications.

General Features

N-channel

- V_{DS} = 40 V,I_D = 6 A

  $R_{DS(ON)}$ < 38 mΩ @ V_{GS}=10V

  $R_{DS(ON)}$ < 63 mΩ @ V_{GS}=4.5V

P-channel

- V_{DS} = -40 V,I_D = -6.5 A

  $R_{DS(ON)}$ < 34 mΩ @ V_{GS}=-10V

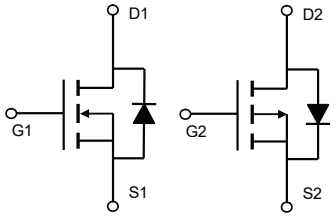
  $R_{DS(ON)}$ < 53 mΩ @ V_{GS}=-4.5V

- High density cell design for ultra low $R_{DS(ON)}$
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation
- 100% Rg tested
- 100% ΔVds tested
- 100% UIS tested

Application

- H-bridge
- Inverters

SOP-8



Schematic

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
VSM6NP04	VSM6NP04-S8	SOP-8	Ø330mm	12mm	4000units

Absolute Maximum Ratings (T_A=25℃unless otherwise noted)

Parameter	Symbol	N-Channel	P-Channel	Unit
Drain-Source Voltage	V_{DS}	40	-40	V
Gate-Source Voltage	V_{GS}	±20	±20	V
Continuous Drain Current	I_D	6	-6.5	A
Continuous Drain Current(T_A=75℃)	I_D(75℃)	4.6	-5	A
Pulsed Drain Current	I_{DM}	24	-26	A
Maximum Power Dissipation	P_D	2	2	W
Single pulse avalanche energy (Note 1)	E_{AS}	31	15	mJ

Operating Junction and Storage Temperature Range	T_J,T_{STG}	-55 To 150	℃

Thermal Characteristic

Thermal Resistance,Junction-to-Case (Note 2)**(N-channel)**	$R_{\theta JC}$	30	℃/W
Thermal Resistance,Junction-to-Case (Note 2)**(P-channel)**	$R_{\theta JC}$	30	℃/W
Thermal Resistance,Junction-to-Ambient (Note 3)**(N-channel)**	$R_{\theta JA}$	62.5	℃/W
Thermal Resistance,Junction-to-Ambient (Note 3)**(P-channel)**	$R_{\theta JA}$	62.5	℃/W

N-Channel Electrical Characteristics (T_A=25℃unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=250μA	40	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=40V,V_{GS}=0V	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V	-	-	±100	nA
On Characteristics						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA	1	1.6	2.2	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=6A	-	33	38	mΩ
		V_{GS}=4.5V, I_D=3A	-	48	63	mΩ
Forward Transconductance	g_{FS}	V_{DS}=5V,I_D=6A	-	8	-	S
Dynamic Characteristics						
Input Capacitance	C_{lss}	V_{DS}=20V,V_{GS}=0V, F=1.0MHz	-	280	-	pF
Output Capacitance	C_{oss}		-	46	-	pF
Reverse Transfer Capacitance	C_{rss}		-	34	-	pF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=20V ,R_L=3.3Ω V_{GS}=10V,R_G=3Ω	-	6	-	nS
Turn-on Rise Time	t_r		-	4	-	nS
Turn-off Delay Time	$t_{d(off)}$		-	16	-	nS
Turn-off Fall Time	t_f		-	8	-	nS
Total Gate Charge	Q_g	V_{DS}=20V,I_D=6A, V_{GS}=10V	-	10.2	-	nC
Gate-Source Charge	Q_{gs}		-	1.9	-	nC
Gate-Drain Charge	Q_{gd}		-	2.1	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage	V_{SD}	V_{GS}=0V,I_S=3A	-	-	1.2	V
Diode Forward Current	I_S		-	-	6	A

P-Channel Electrical Characteristics (T_A=25℃unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=-250μA	-40	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-40V,V_{GS}=0V	-	-	-1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V	-	-	±100	nA
On Characteristics						

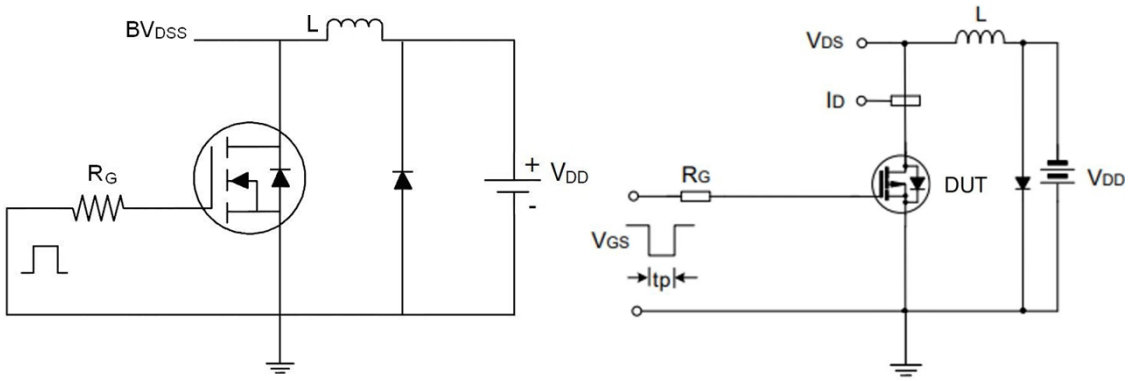
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=-250μA	-1.0	-1.7	-2.2	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=-10V, I_D=-7A	-	28	34	mΩ
		V_{GS}=-4.5V, I_D=-4A	-	39	53	mΩ
Forward Transconductance	g_{FS}	V_{DS}=-5V,I_D=-7A	-	10	-	S
Dynamic Characteristics						
Input Capacitance	C_{lss}	V_{DS}=-20V,V_{GS}=0V, F=1.0MHz	-	616	-	pF
Output Capacitance	C_{oss}		-	79	-	pF
Reverse Transfer Capacitance	C_{rss}		-	68	-	pF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=-20V ,R_L=2.9Ω V_{GS}=-10V,R_G=3Ω	-	7	-	nS
Turn-on Rise Time	t_r		-	5	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	19	-	nS
Turn-Off Fall Time	t_f		-	6	-	nS
Total Gate Charge	Q_g	V_{DS}=-20V,I_D=-7A V_{GS}=-10V	-	17.2	-	nC
Gate-Source Charge	Q_{gs}		-	2.3	-	nC
Gate-Drain Charge	Q_{gd}		-	4.7	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage	V_{SD}	V_{GS}=0V,I_S=-4A	-	-	-1.2	V
Diode Forward Current	I_S		-	-	-6.5	A

Notes:

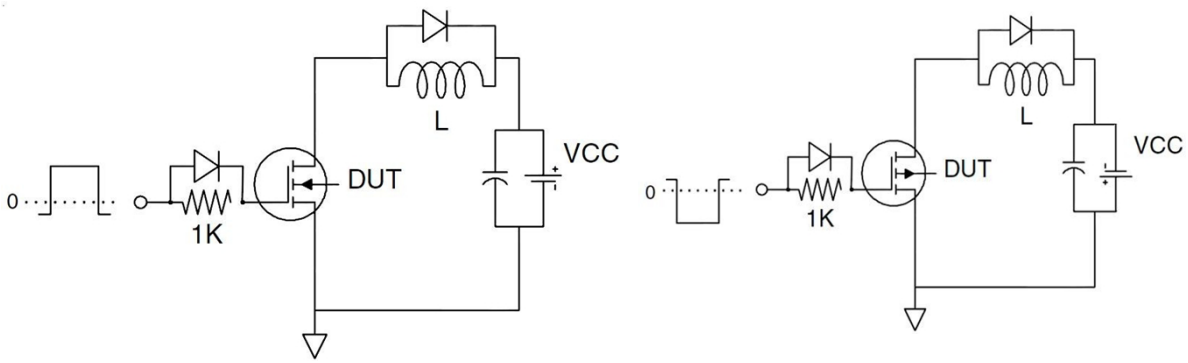
1. EAS condition : Tj=25℃,V_{DD}={20V(N-Channel),-20V(P-Channel)},V_G={10V(N-Channel),-10V(P-Channel)},L=0.5mH,Rg=25Ω.
2. The $R_{\theta JC}$ is the thermal impedance from junction to lead.
3. The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C. The maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design, and the maximum temperature of 150°C may be used if the PCB allows it.
4. Guaranteed by design, not subject to production.
5. These curves are based on the junction-to-ambient thermal impedance, assuming a maximum junction temperature of $T_{J(MAX)}$=150°C. The SOA curve provides a single pulse rating.

Test Circuit

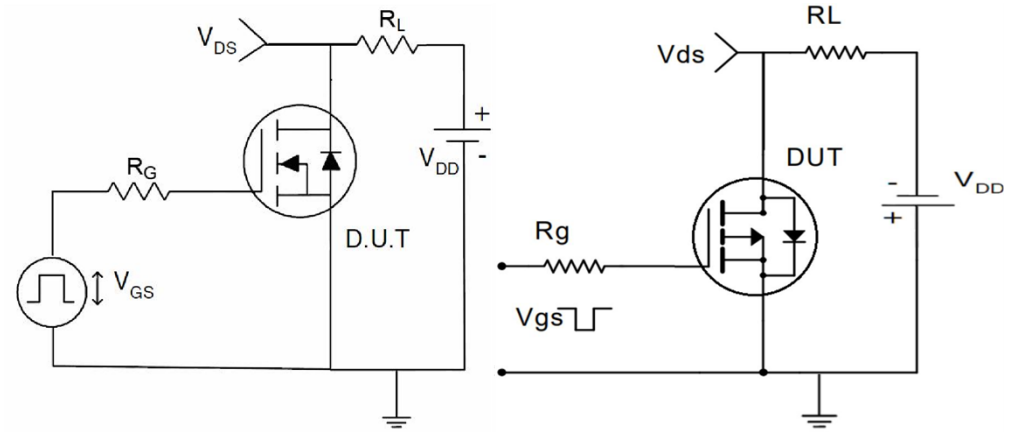
1) E_{AS} Test Circuit



2) Gate Charge Test Circuit



3) Switch Time Test Circuit



N-Channel Typical Electrical and Thermal Characteristics (Curves)

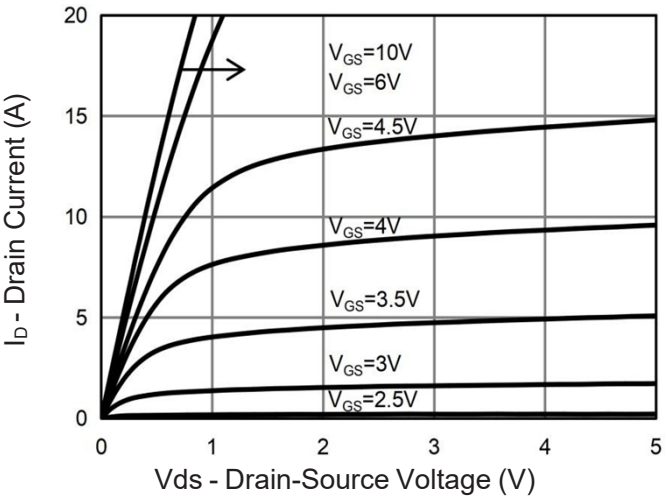


Figure 1 Output Characteristics

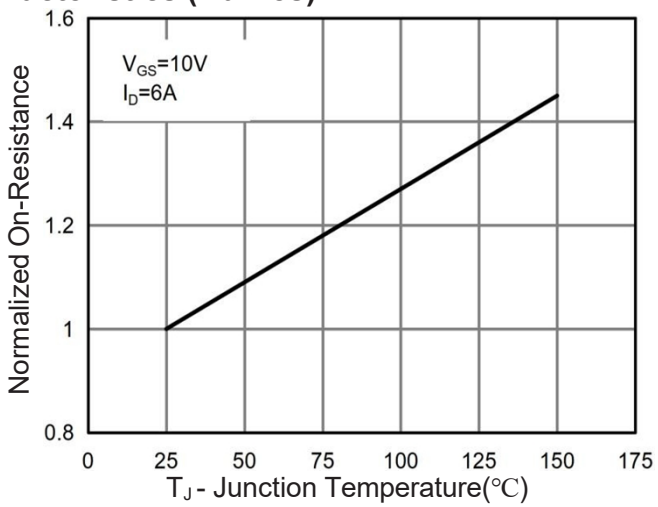


Figure 4 Rdson vs Junction Temperature

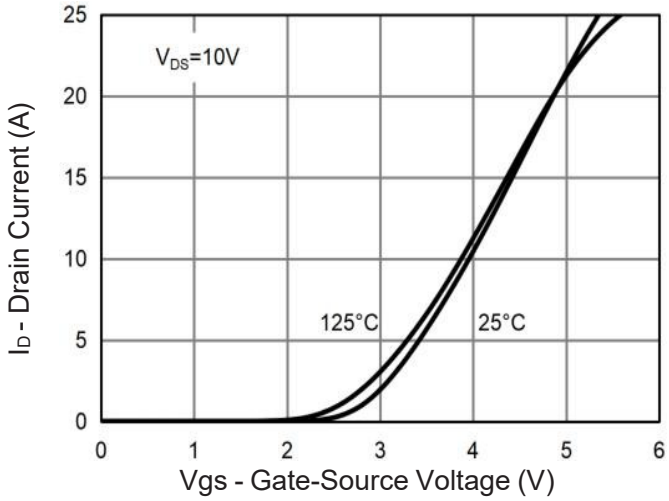


Figure 2 Transfer Characteristics

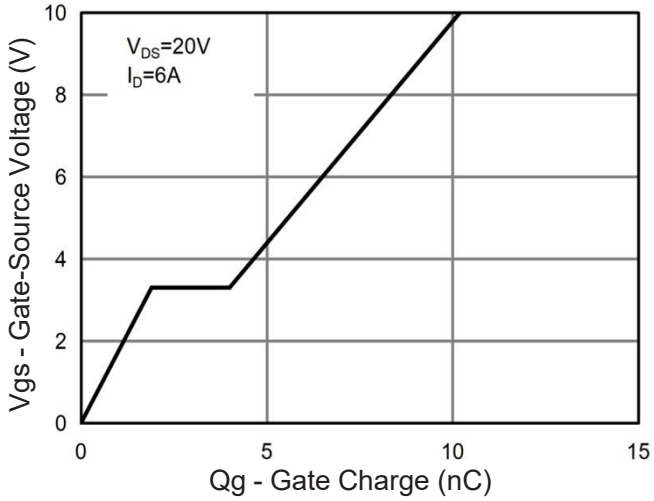


Figure 5 Gate Charge

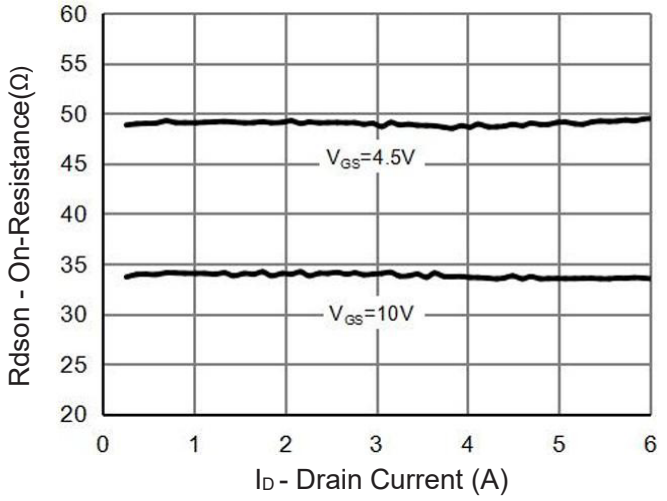


Figure 3 Rdson vs Drain Current

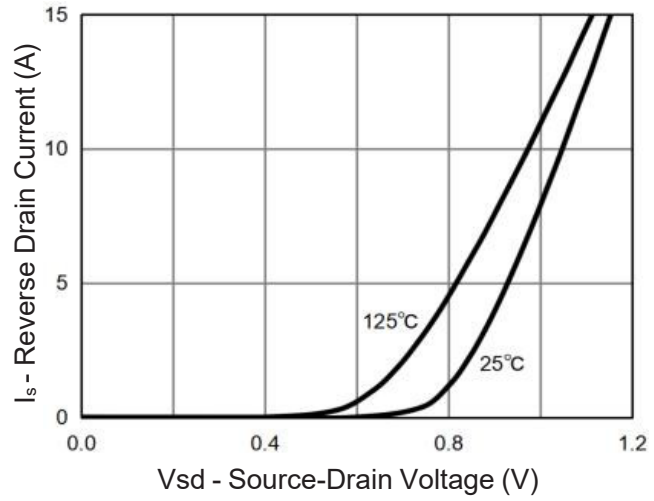


Figure 6 Source-Drain Diode Forward

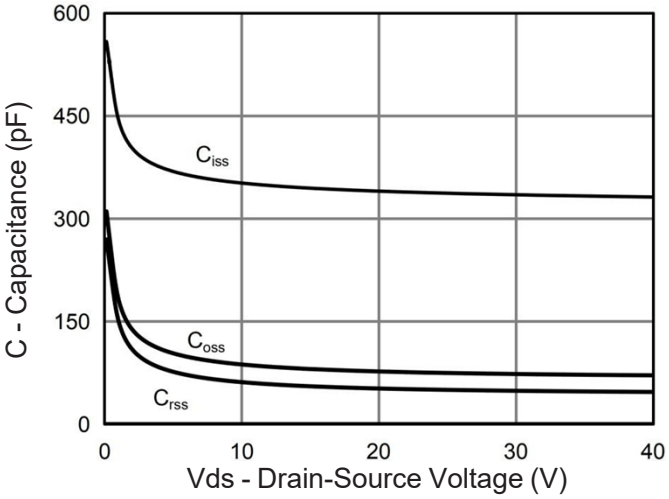


Figure 7 Capacitance vs Vds

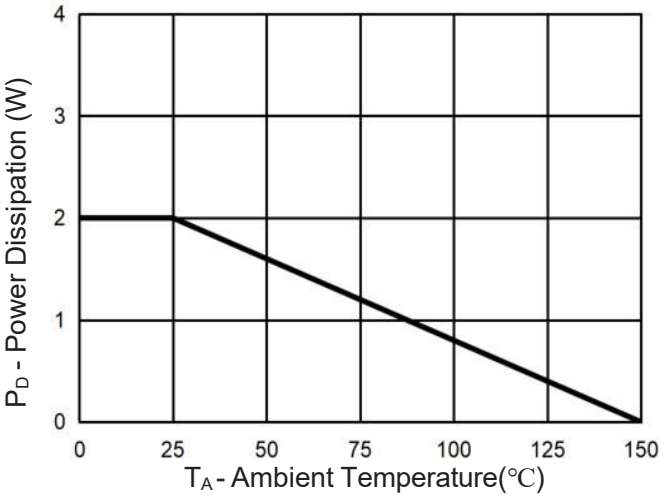


Figure 9 Power De-rating

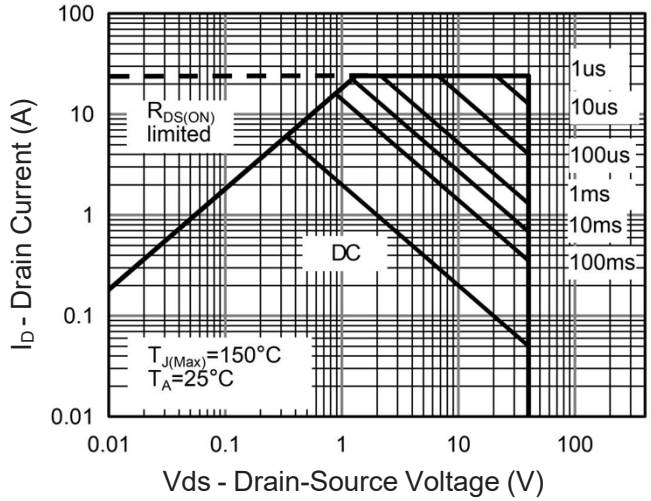


Figure 8 Safe Operation Area (Note 5)

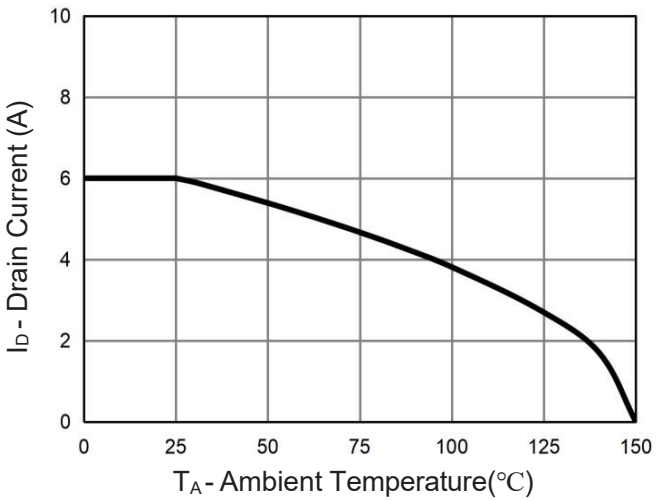


Figure 10 Drain Current De-rating

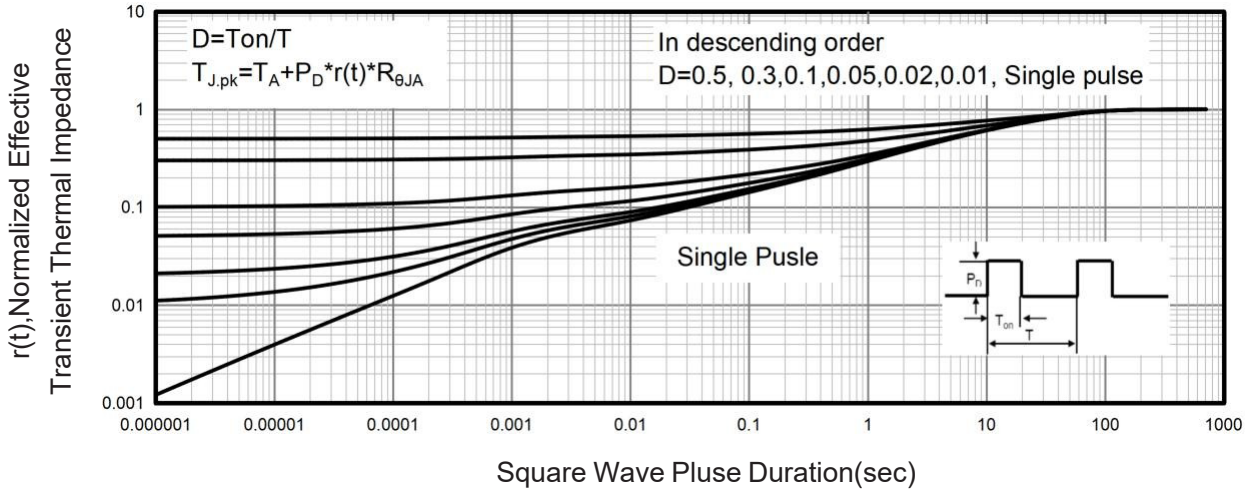


Figure 11 Normalized Maximum Transient Thermal Impedance

P-Channel Typical Electrical and Thermal Characteristics (Curves)

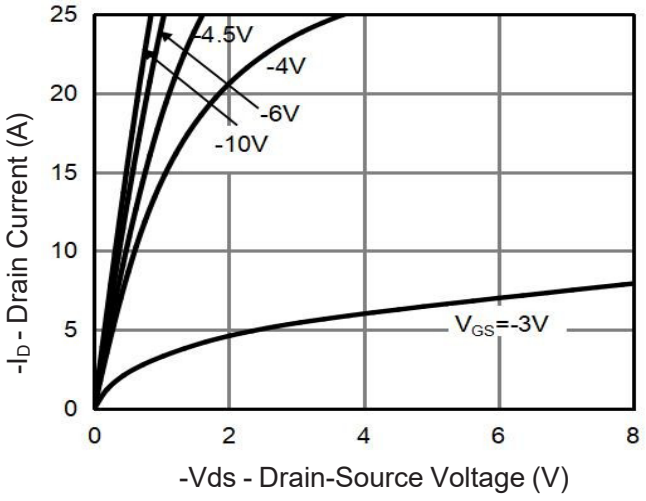


Figure 1 Output Characteristics

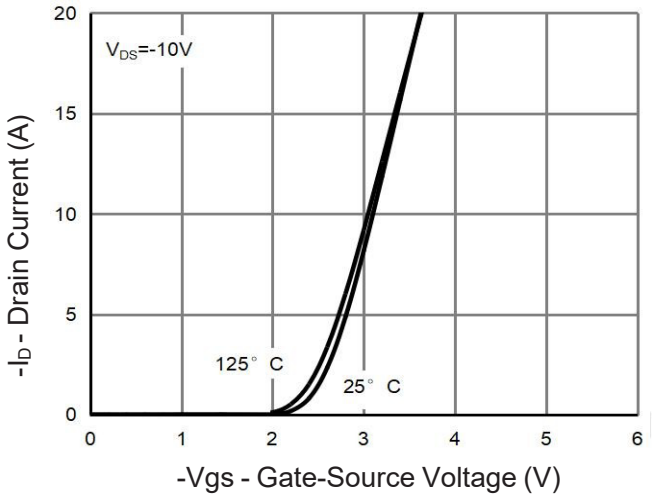


Figure 2 Transfer Characteristics

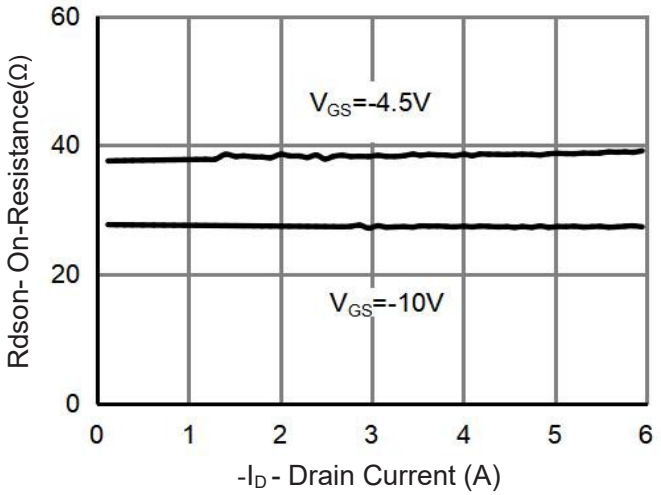


Figure 3 Rdson vs Drain Current

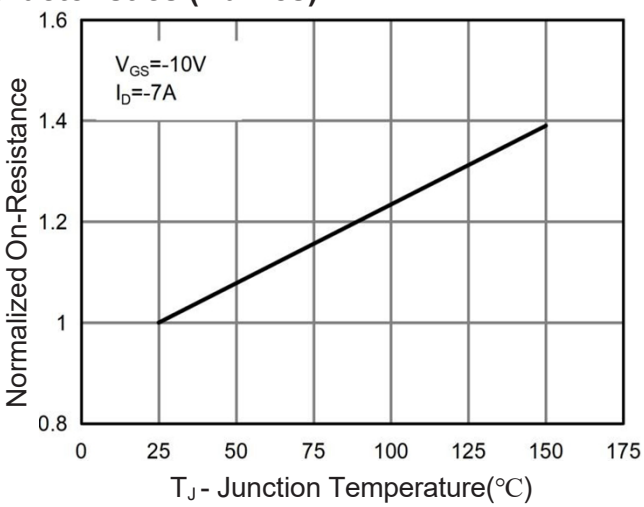


Figure 4 Rdson vs Junction Temperature

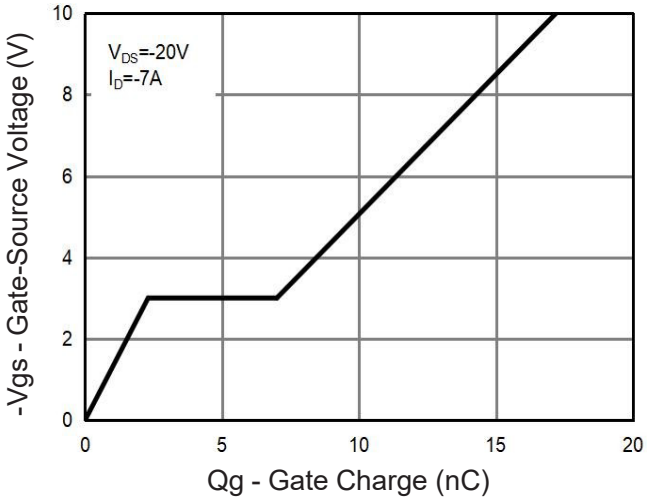


Figure 5 Gate Charge

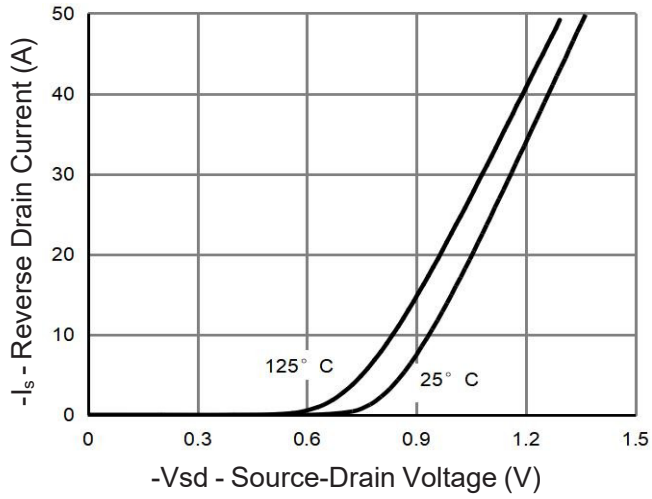


Figure 6 Source-Drain Diode Forward

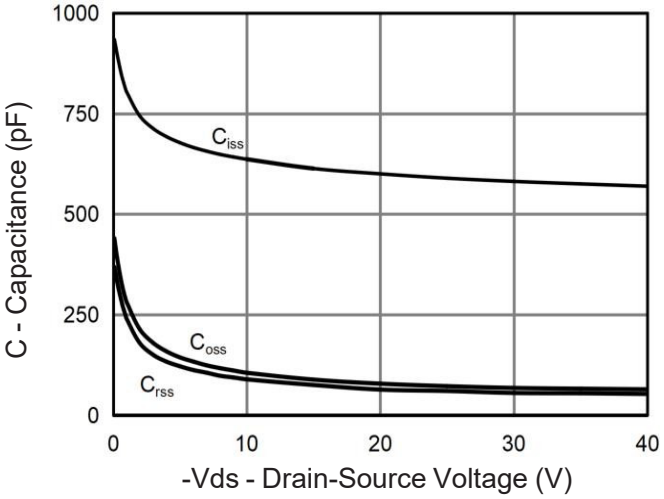


Figure 7 Capacitance vs Vds

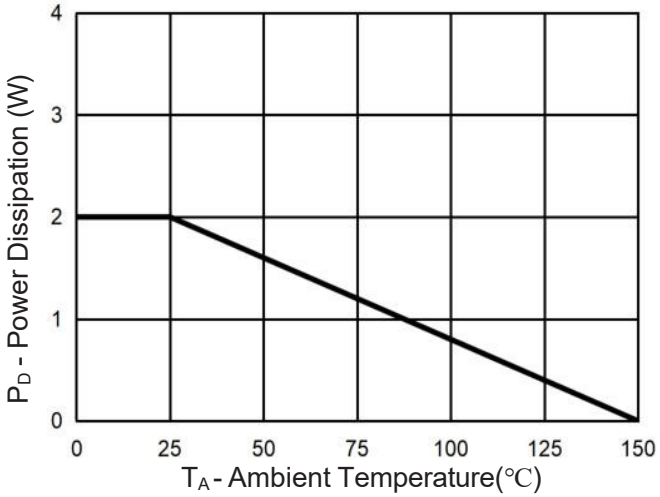


Figure 9 Power De-rating

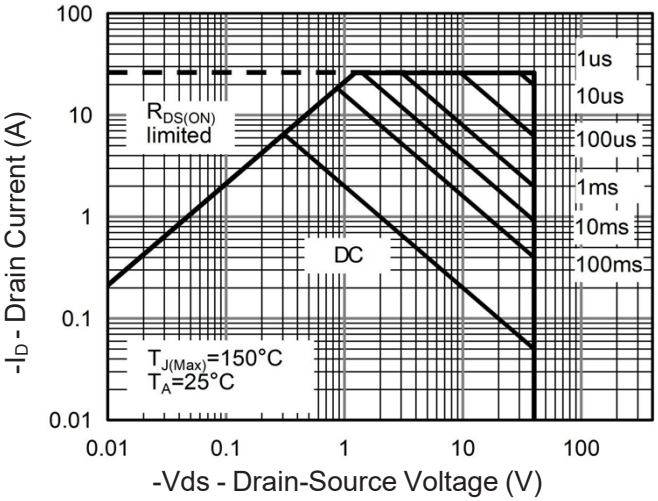


Figure 8 Safe Operation Area (Note 5)

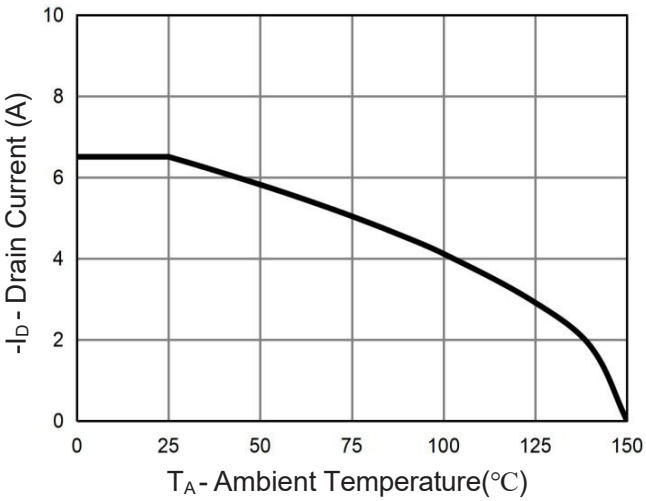


Figure 10 Drain Current De-rating

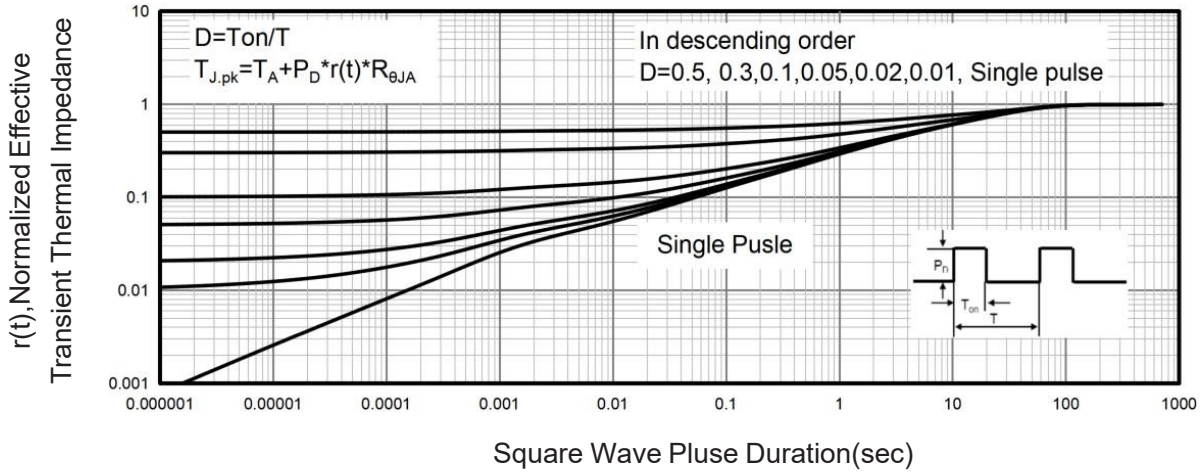


Figure 11 Normalized Maximum Transient Thermal Impedance