

Description

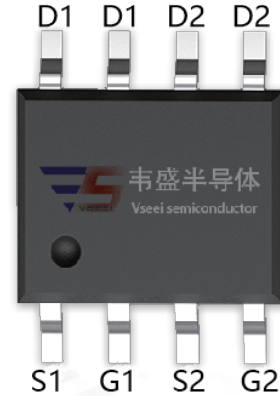
The VSM5DN06 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

General Features

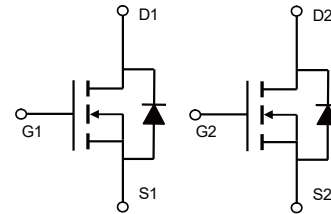
- $V_{DS}=60V, I_D=5A$
 $R_{DS(ON)} < 30m\Omega @ V_{GS}=10V$ (Typ.26m Ω)
 $R_{DS(ON)} < 38m\Omega @ V_{GS}=4.5V$ (Typ.32m Ω)
- High density cell design for ultra low R_{dson}
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation
- 100% Rg tested
- 100% ΔV_{ds} tested
- 100% UIS tested

Application

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply



SOP-8



Schematic

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
VSM5DN06	VSM5DN06-S8	SOP-8	Ø330mm	12mm	4000 units

Absolute Maximum Ratings ($T_A=25^{\circ}C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	5	A
Drain Current-Continuous($T_A=100^{\circ}C$)	$I_D(100^{\circ}C)$	3.5	A
Pulsed Drain Current	I_{DM}	24	A
Maximum Power Dissipation	P_D	2	W
Single pulse avalanche energy (Note 5)	E_{AS}	65	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	$^{\circ}C$

Thermal Characteristic

Thermal Resistance, Junction-to-Ambient (Note 2)	$R_{\theta JA}$	62.5	$^{\circ}C/W$
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Electrical Characteristics ($T_A=25^{\circ}\text{C}$ unless otherwise noted)

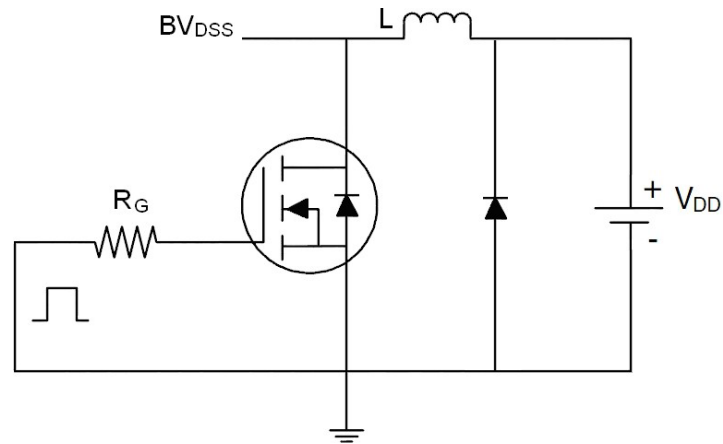
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	60	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=60V, V_{GS}=0V$	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.2	1.6	2.5	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=5A$	-	26	30	m Ω
	$R_{DS(ON)}$	$V_{GS}=4.5V, I_D=5A$	-	32	38	m Ω
Forward Transconductance	g_{FS}	$V_{DS}=5V, I_D=5A$	11	-	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C_{iss}	$V_{DS}=30V, V_{GS}=0V,$ $F=1.0MHz$	-	846	-	pF
Output Capacitance	C_{oss}		-	65	-	pF
Reverse Transfer Capacitance	C_{rss}		-	61.8	-	pF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=30V, R_L=6.7\Omega$ $V_{GS}=10V, R_G=3\Omega$	-	5.2	-	nS
Turn-on Rise Time	t_r		-	3	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	17	-	nS
Turn-Off Fall Time	t_f		-	2.5	-	nS
Total Gate Charge	Q_g	$V_{DS}=30V, I_D=5A,$ $V_{GS}=10V$	-	25		nC
Gate-Source Charge	Q_{gs}		-	3		nC
Gate-Drain Charge	Q_{gd}		-	6.4		nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	$V_{GS}=0V, I_S=5A$	-		1.2	V
Diode Forward Current (Note 2)	I_S		-	-	5	A
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

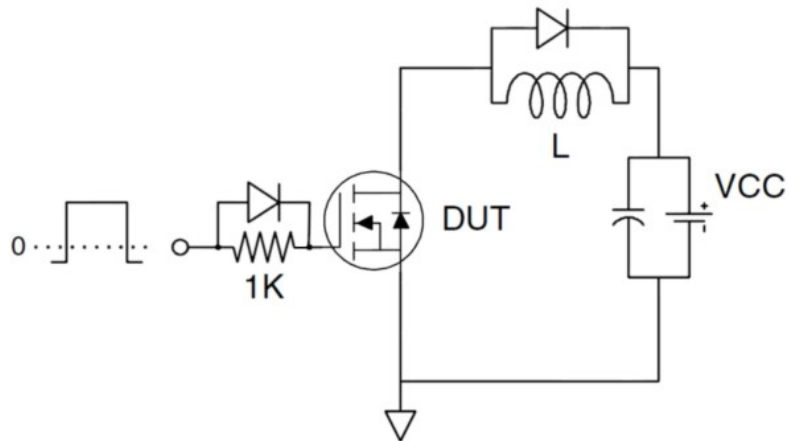
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. EAS condition: $T_J=25^{\circ}\text{C}, V_{DD}=30V, V_G=10V, L=0.5mH, R_g=25\Omega$

Test Circuit

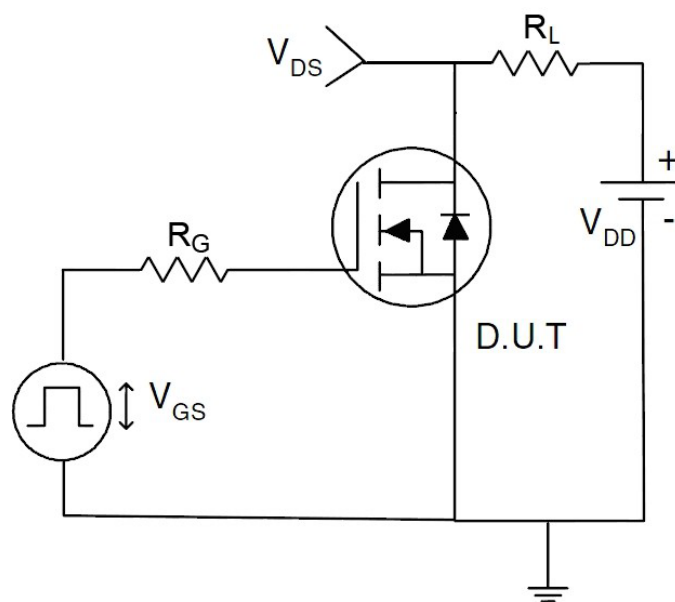
1) E_{AS} test Circuit



2) Gate charge test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

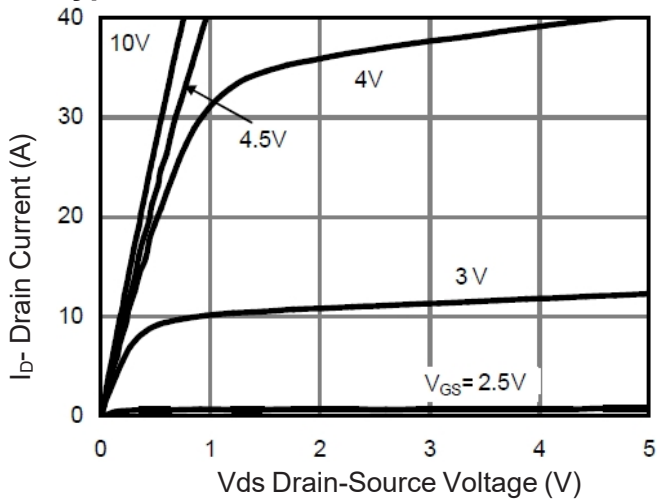


Figure 1 Output Characteristics

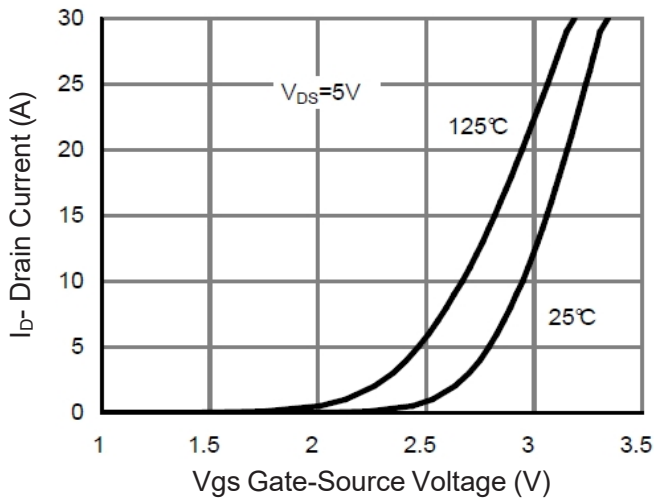


Figure 2 Transfer Characteristics

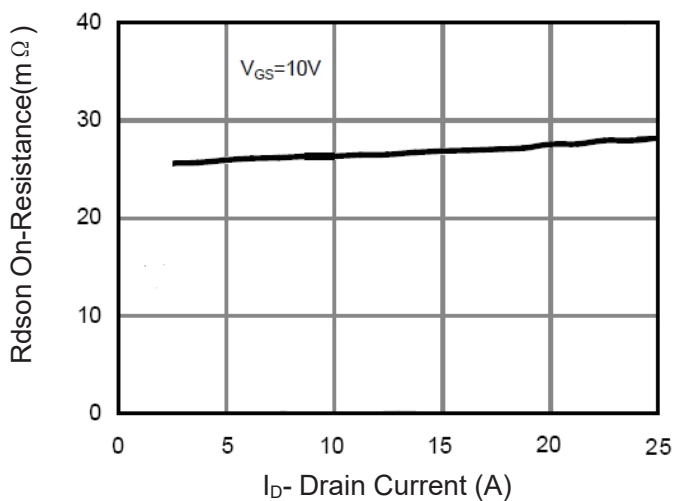


Figure 3 Rdson- Drain Current

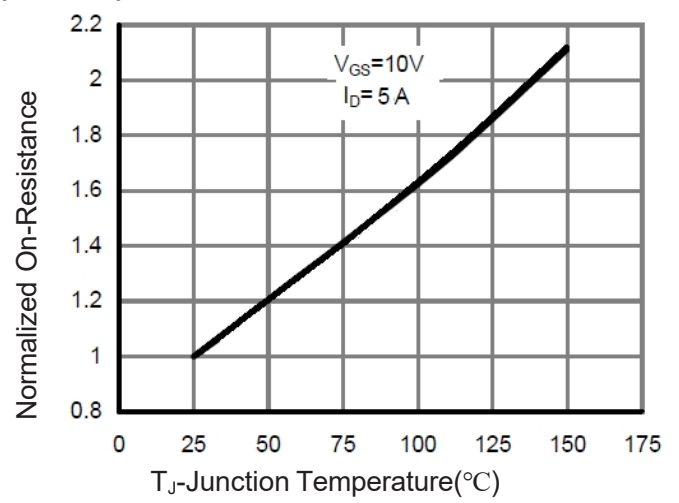


Figure 4 Rdson-Junction Temperature

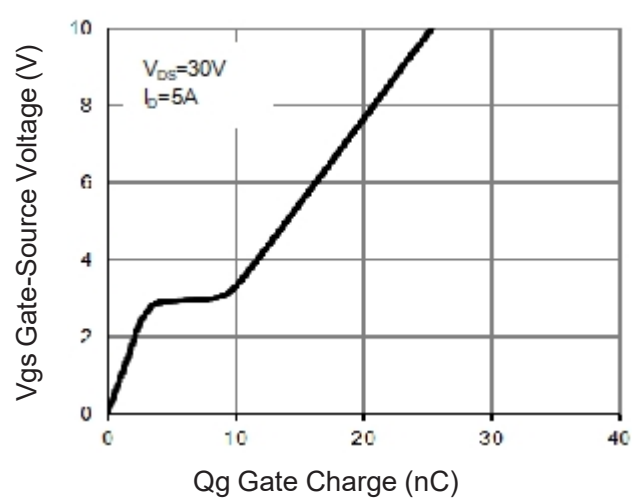


Figure 5 Gate Charge

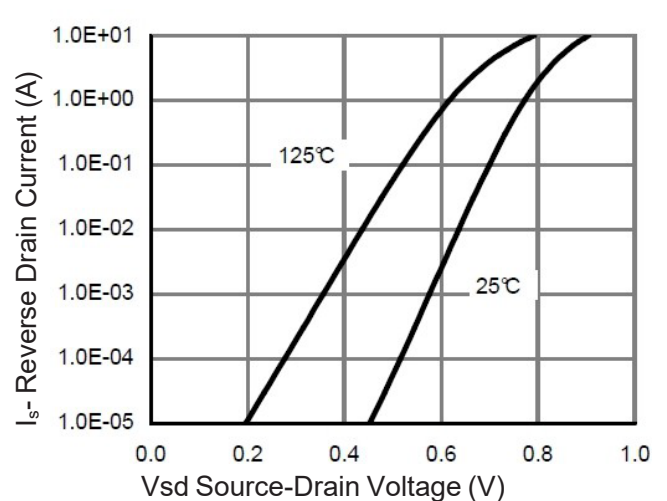
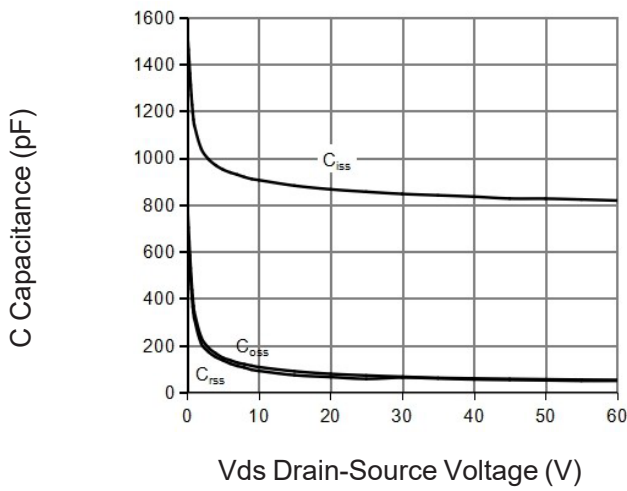
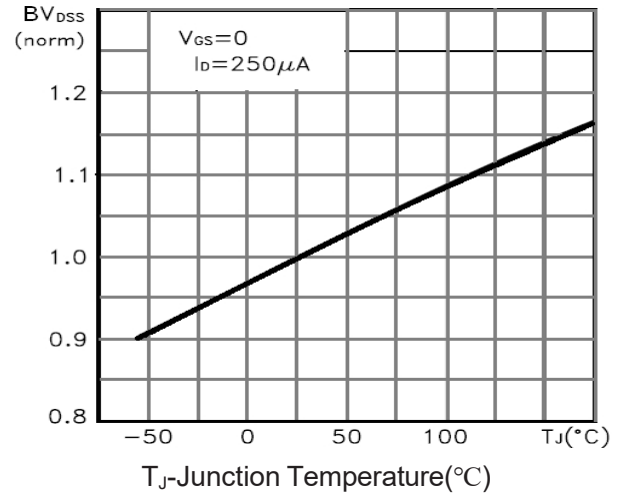
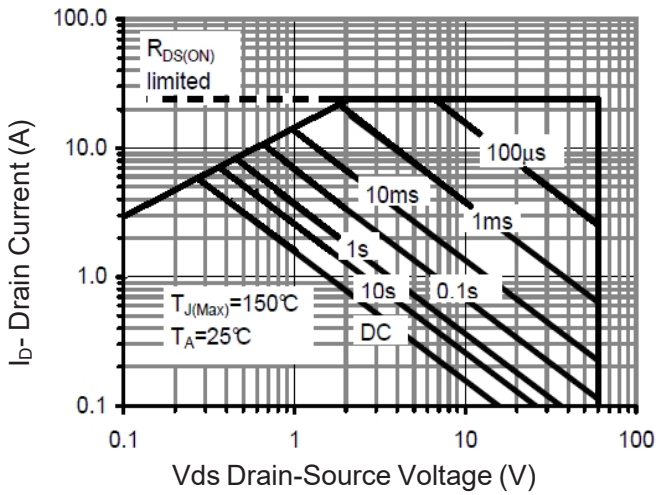
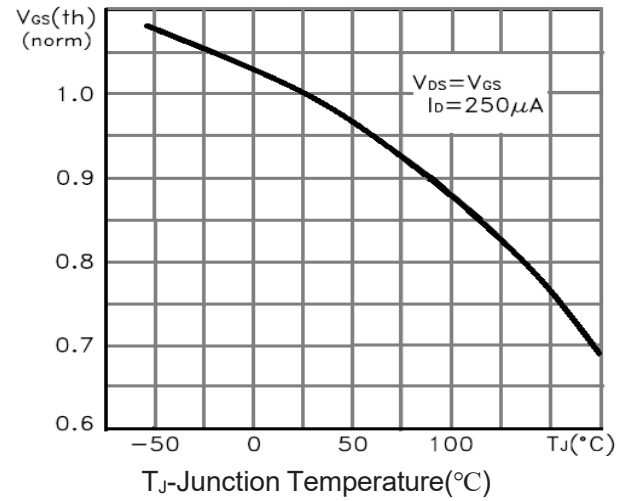
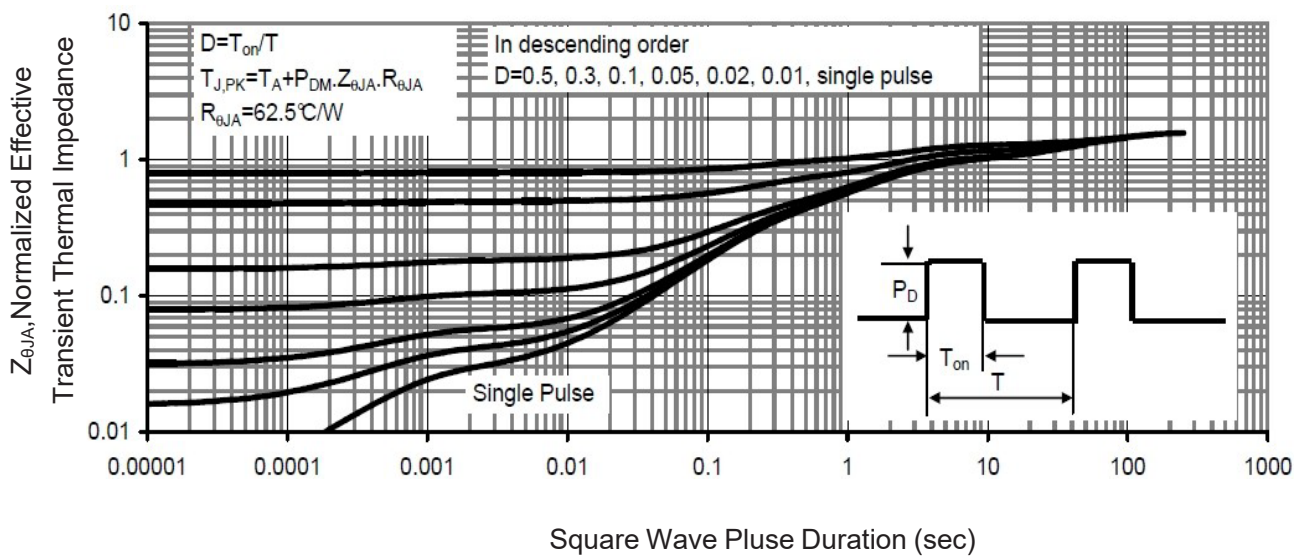


Figure 6 Source- Drain Diode Forward


Figure 7 Capacitance vs Vds

Figure 9 BV_{DSS} vs Junction Temperature

Figure 8 Safe Operation Area

Figure 10 V_{GS(th)} vs Junction Temperature

Figure 11 Normalized Maximum Transient Thermal Impedance