Features

- Excellent $R_{DS(ON)}$ and Low Gate Charge
- 100% UIS Tested
- 100% ΔVds Tested
- Halogen-free; RoHS-compliant

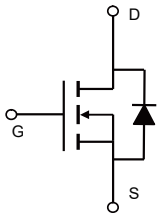
Applications

- Load Switch
- PWM Application
- Power Management

Product Summary

Parameters	Value	Unit
V_{DSS}	600	V
$V_{GS(th)\_Typ}$	3.0	V
I_D(@V_{GS}=10V)	25	A
$R_{DS(ON)\_Typ}$(@V_{GS}=10V	267	mΩ

TO-220F



Schematic

Ordering Information

Device	Marking	MSL	Form	Package	Tube(pcs)	Per Carton (pcs)
VSM25N60-TF	VSM25N60	N/A	Tube	TO-220F	50	5000

Absolute Maximum Ratings (@ T_A = 25°C unless otherwise specified)

Symbol	Parameter		Value	Unit
V_{DS}	Drain-to-Source Voltage		600	V
V_{GS}	Gate-to-Source Voltage		±30	V
I_D	Continuous Drain Current	T_A = 25°C	25	A
		T_A = 100°C	16	
I_{DM}	Pulsed Drain Current (1)		Refer to Fig.4	A
E_{AS}	Single Pulsed Avalanche Energy (2)		1080	mJ
P_D	Power Dissipation	T_A = 25°C	9	W
		T_A = 100°C	4	
T_J, T_{STG}	Junction & Storage Temperature Range		-55 to 150	°C

Thermal Characteristics

Symbol	Parameter	Max	Unit
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient(3)	61	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient(4)	14	

Electrical Characteristics (T_J = 25°C unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0V	600	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 600V, V_{GS} = 0V	-	-	1.0	μA
I_{GSS}	Gate-Body Leakage Current	V_{DS} = 0V, V_{GS} = ±30V	-	-	±100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 μA	2.1	3.0	3.9	V
$R_{DS(ON)}$	Static Drain-Source ON-Resistance(5)	V_{GS} = 10V, I_D = 15A	-	267	347	mΩ
Dynamic Characteristics						
R_g	Gate Resistance	f = 1MHz	-	1.9	-	Ω
C_{iss}	Input Capacitance	V_{GS} = 0V, V_{DS} = 300V, f = 1MHz	2907	4070	5494	pF
C_{oss}	Output Capacitance		66	92	124	pF
C_{rss}	Reverse Transfer Capacitance		11	16	21	pF
Q_g	Total Gate Charge	V_{GS} = 0 to 10V V_{DS} = 300V, I_D = 25A	61	85	115	nC
Q_{gs}	Gate Source Charge		16	23	31	nC
Q_{gd}	Gate Drain("Miller") Charge		20	28	38	nC
Switching Characteristics						
$t_{d(on)}$	Turn-On DelayTime	V_{GS} = 10V, V_{DD} = 300V I_D= 25A, R_{GEN} = 6.2Ω	-	23	-	ns
t_r	Turn-On Rise Time		-	43	-	ns
$t_{d(off)}$	Turn-Off DelayTime		-	87	-	ns
t_f	Turn-Off Fall Time		-	49	-	ns
Body Diode Characteristics						
I_S	Maximum Continuous Body Diode Forward Current		-	-	25	A
I_{SM}	Maximum Pulsed Body Diode Forward Current		-	-	100	A
V_{SD}	Body Diode Forward Voltage	V_{GS} = 0V, I_S = 15A	-		1.2	V
trr	Body Diode Reverse Recovery Time	I_F = 25A, di/dt = 100A/us	449	629	850	ns
Qrr	Body Diode Reverse Recovery Charge		-	8948	-	nC

Notes:

1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature.
2. E_{AS} condition: Starting T_J=25C, V_{DD}=100V, V_{GS}=10V, R_G=25ohm, L=10mH, I_{AS}=14.7A, V_{DD}=0V during time in avalanche.
3. $R_{\theta JA}$ is measured with the device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.
4. $R_{\theta JA}$ is measured with the device mounted on a 1inch^2 pad of 2oz copper FR4 PCB.
5. Pulse Test: Pulse Width≤300μs, Duty Cycle≤0.5%.

Typical Performance Characteristics

Figure 1: Power De-rating

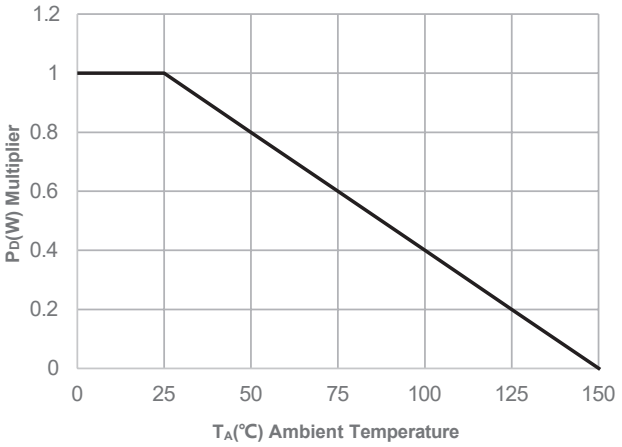


Figure 2: Current De-rating

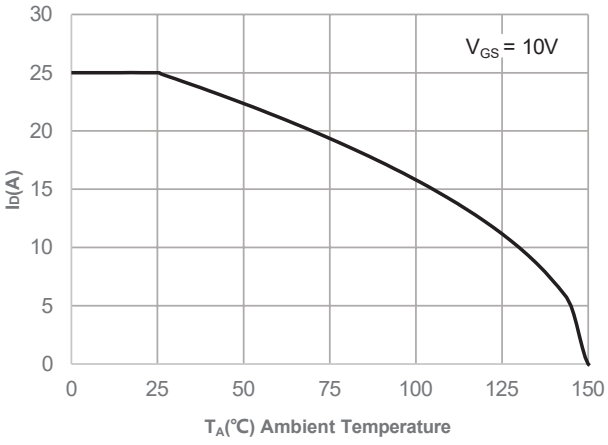


Figure 3: Normalized Maximum Transient Thermal Impedance

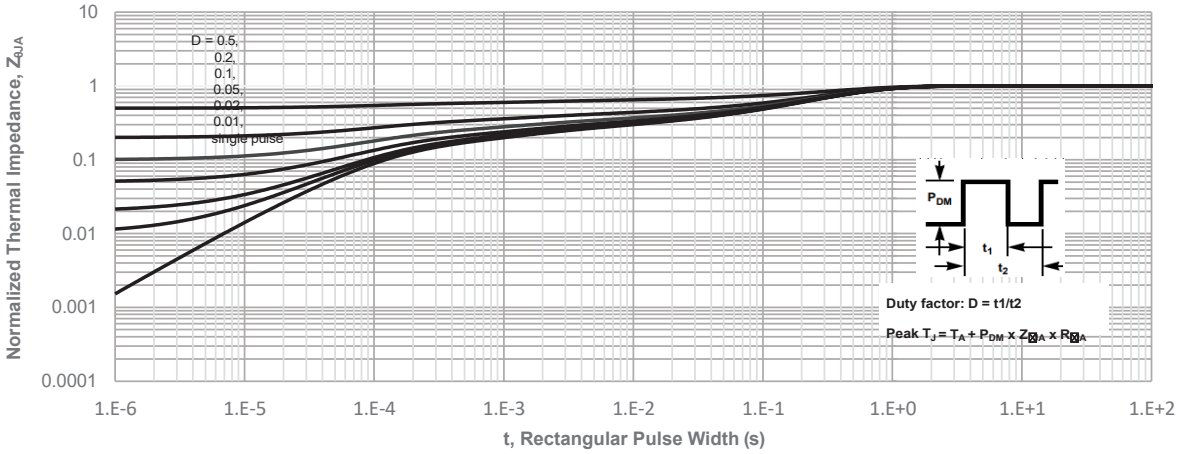
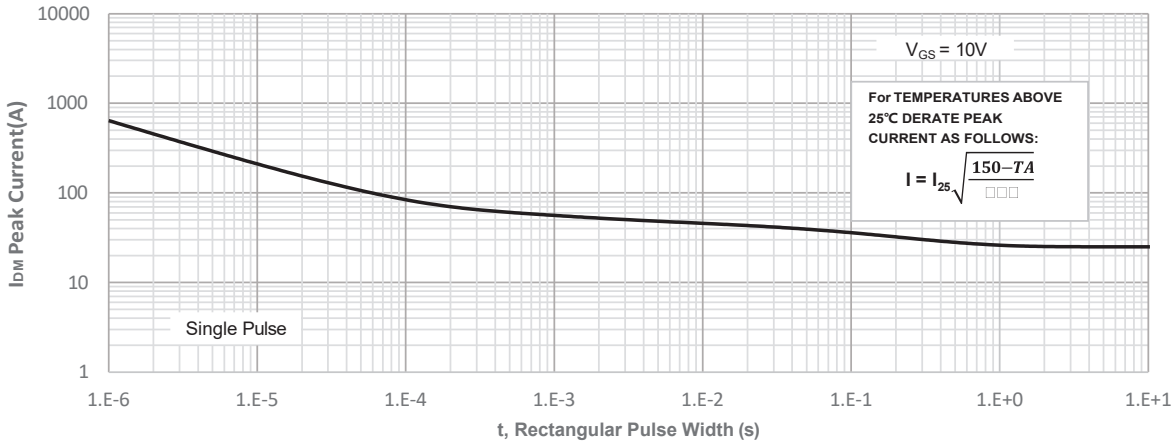


Figure 4: Peak Current Capacity



Typical Performance Characteristics

Figure 5: Output Characteristics

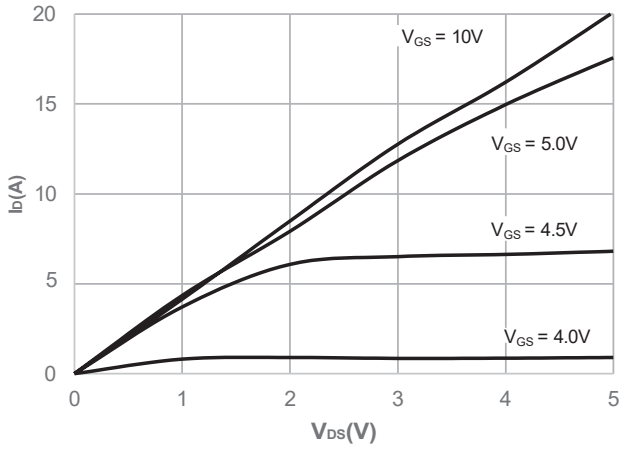


Figure 6: Typical Transfer Characteristics

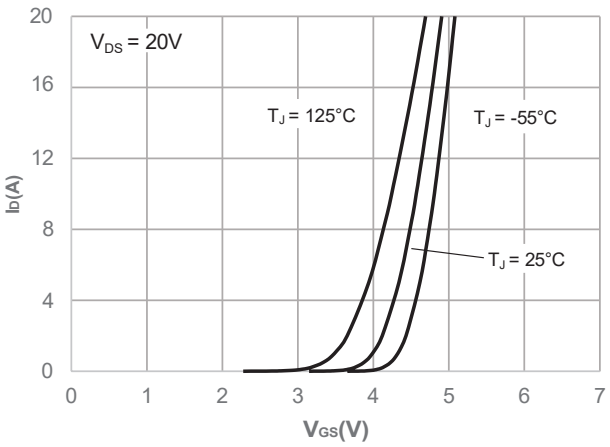


Figure 7: On-resistance vs. Drain Current

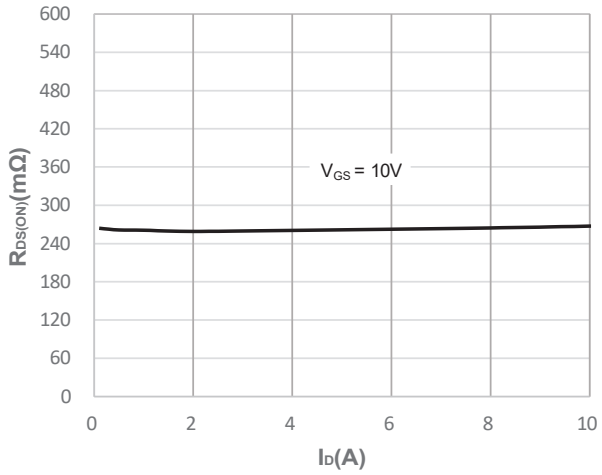


Figure 8: Body Diode Characteristics

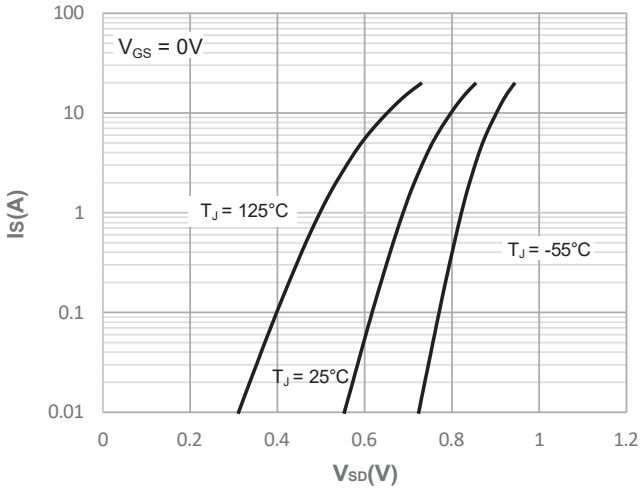


Figure 9: Gate Charge Characteristics

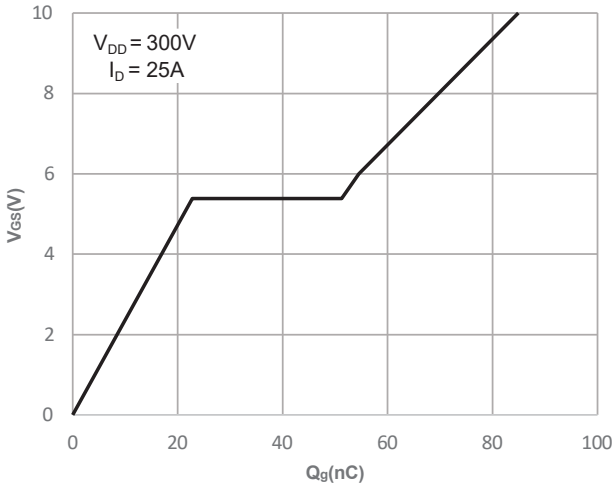
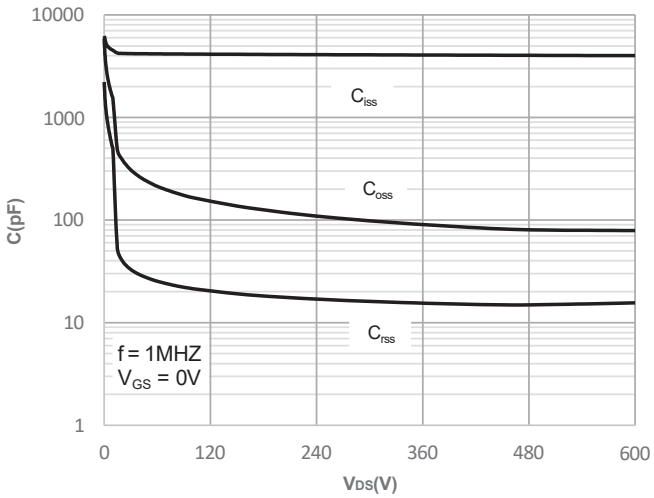


Figure 10: Capacitance Characteristics



Typical Performance Characteristics

Figure 11: Normalized Breakdown voltage vs. Junction Temperature

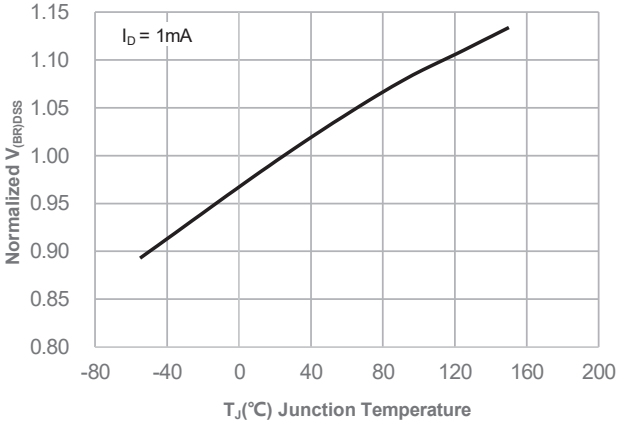


Figure 12: Normalized on Resistance vs. Junction Temperature

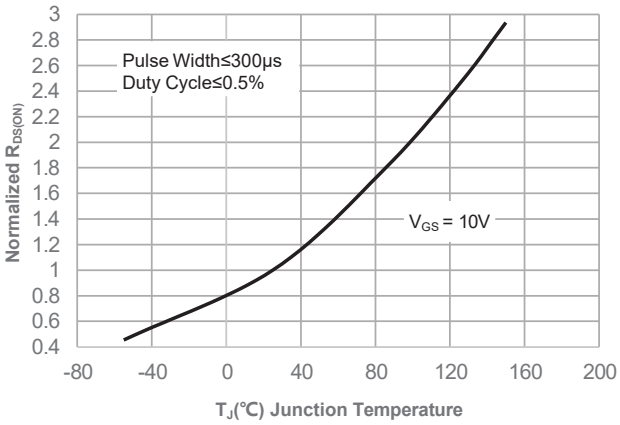


Figure 13: Normalized Threshold Voltage vs. Junction Temperature

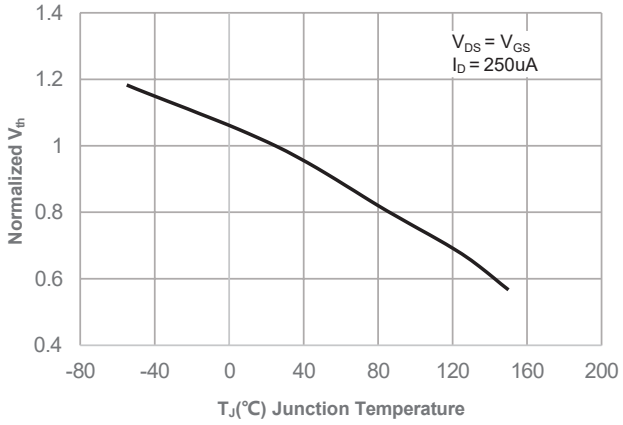


Figure 14: $R_{DS(ON)}$ vs. V_{GS}

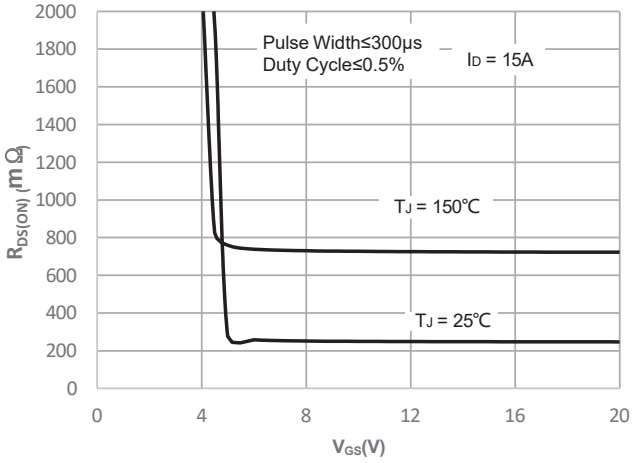
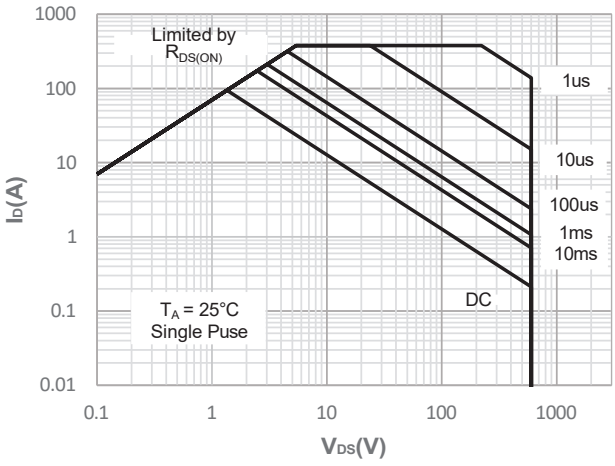


Figure 15: Maximum Safe Operating Area



Test Circuit

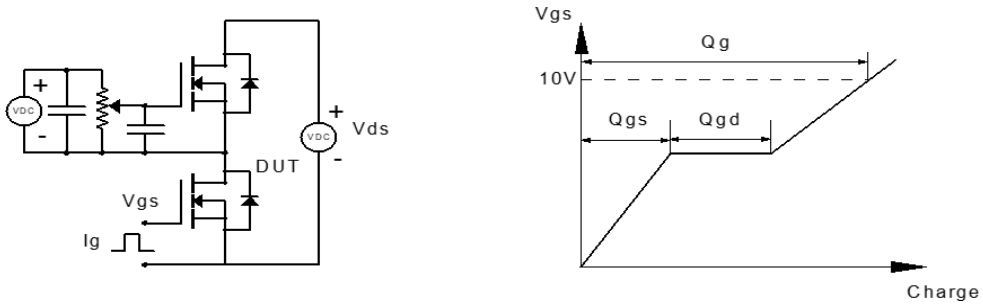


Figure 1: Gate Charge Test Circuit & Waveform

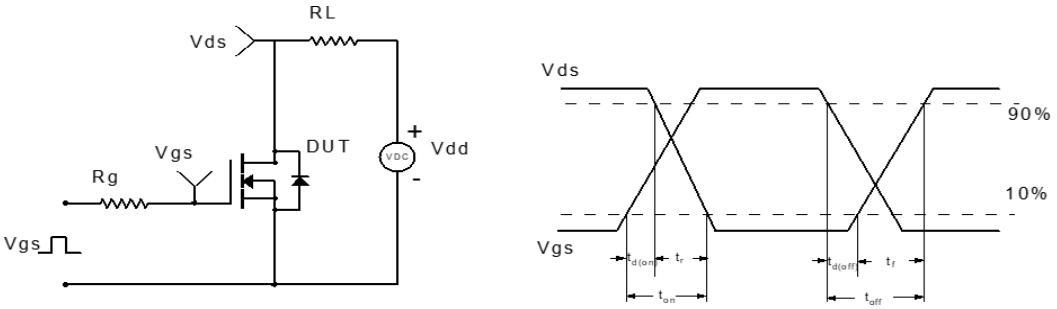


Figure 2: Resistive Switching Test Circuit & Waveform

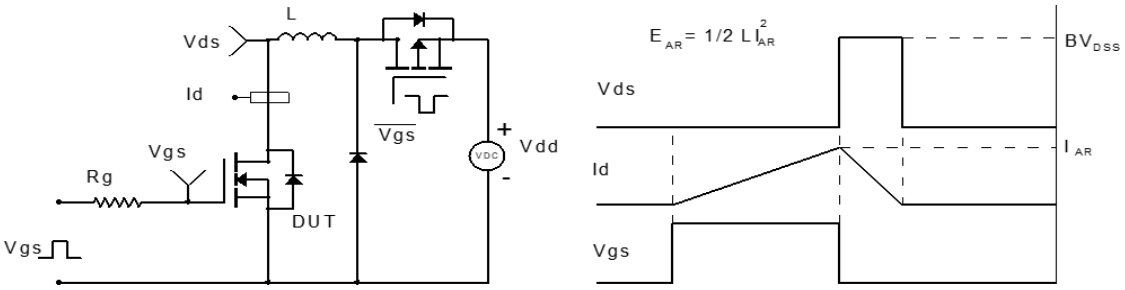


Figure 3: Unclamped Inductive Switching Test Circuit& Waveform

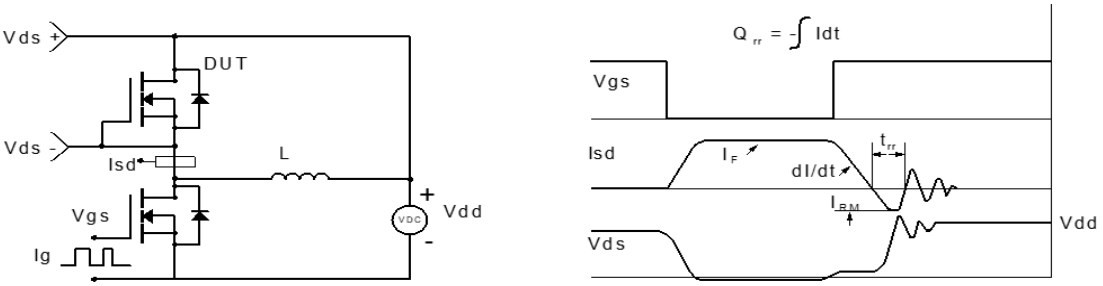


Figure 4: Diode Recovery Test Circuit & Waveform