Features

- Excellent $R_{DS(ON)}$ and Low Gate Charge
- 100% UIS Tested
- 100% ΔVds Tested
- Halogen-free; RoHS-compliant

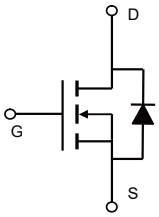
Applications

- SMPS with PFC
- Flyback and LLC topologies
- Silver ATX,adapter,TV,lighting,Telecom

Product Summary

Parameters	Value	Unit
V_{DSS}	650	V
$V_{GS(th)\_Typ}$	3.1	V
I_D(@V_{GS}=10V)	9	A
$R_{DS(ON)\_Typ}$(@V_{GS}=10V	578	mΩ

TO-252



Schematic

Ordering Information

Device	Marking	MSL	Form	Package	Reel(pcs)	Per Carton (pcs)
VSM9N65-T2	VSM9N65	3	Tape&Reel	TO-252	2500	25000

Absolute Maximum Ratings (@ T_C = 25°C unless otherwise specified)

Symbol	Parameter		Value	Unit
V_{DS}	Drain-to-Source Voltage		650	V
V_{GS}	Gate-to-Source Voltage		±30	V
I_D	Continuous Drain Current	T_C = 25°C	9	A
		T_C = 100°C	6	
I_{DM}	Pulsed Drain Current (1)		Refer to Fig.4	A
E_{AS}	Single Pulsed Avalanche Energy (2)		120	mJ
P_D	Power Dissipation	T_C = 25°C	46	W
		T_C = 100°C	19	
T_J, T_{STG}	Junction & Storage Temperature Range		-55 to 150	°C

Thermal Characteristics

Symbol	Parameter	Max	Unit
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient(3)	55	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction to Case	2.7	

Electrical Characteristics (T_J = 25°C unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0V	650	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 650V, V_{GS} = 0V	-	-	1.0	μA
I_{GSS}	Gate-Body Leakage Current	V_{DS} = 0V, V_{GS} = ±20V	-	-	±100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 μA	2.2	3.1	4.1	V
$R_{DS(ON)}$	Static Drain-Source ON-Resistance(4)	V_{GS} = 10V, I_D = 3.5A	-	578	650	mΩ
Dynamic Characteristics						
R_g	Gate Resistance	f = 1MHz	-	7.7	-	Ω
C_{iss}	Input Capacitance	V_{GS} = 0V, V_{DS} = 325V, f = 1MHz	342	479	647	pF
C_{oss}	Output Capacitance		15	20.9	28	pF
C_{rss}	Reverse Transfer Capacitance		-	5.0	-	pF
Q_g	Total Gate Charge	V_{GS} = 0 to 10V V_{DS} = 325V, I_D = 10A	-	13	-	nC
Q_{gs}	Gate Source Charge		-	4	-	nC
Q_{gd}	Gate Drain("Miller") Charge		-	5	-	nC
Switching Characteristics						
$t_{d(on)}$	Turn-On DelayTime	V_{GS} = 10V, V_{DD} = 325V I_D= 10A, R_{GEN} = 32.5Ω	-	17	-	ns
t_r	Turn-On Rise Time		-	38	-	ns
$t_{d(off)}$	Turn-Off DelayTime		-	49	-	ns
t_f	Turn-Off Fall Time		-	27	-	ns
Body Diode Characteristics						
I_S	Maximum Continuous Body Diode Forward Current		-	-	9	A
I_{SM}	Maximum Pulsed Body Diode Forward Current		-	-	37	A
V_{SD}	Body Diode Forward Voltage	V_{GS} = 0V, I_S = 3.5A	-		1.2	V
trr	Body Diode Reverse Recovery Time	I_F = 20A, di/dt = 100A/us	258	361	488	ns
Qrr	Body Diode Reverse Recovery Charge		-	4758	-	nC

Notes:

1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature.
2. E_{AS} condition: Starting T_J=25C, V_{DD}=325V, V_G=10V, R_G=25ohm, L=10mH, I_{AS}=4.9A, V_{DD}=0V during time in avalanche.
3. $R_{\theta JA}$ is measured with the device mounted on a FR-4 substrate PC board, 2oz copper, with 1inch square pad layout.
4. Pulse Test: Pulse Width≤300μs, Duty Cycle≤0.5%.

Typical Performance Characteristics

Figure 1: Power De-rating

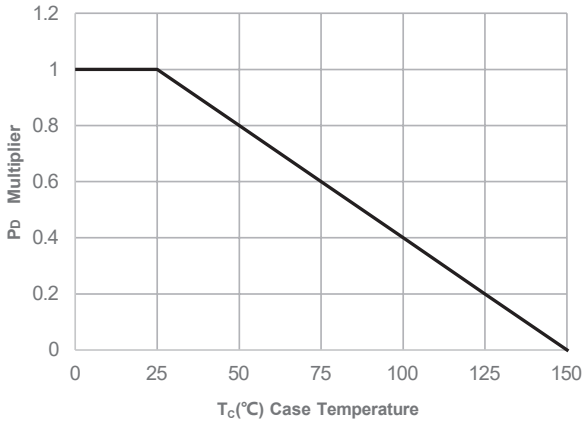


Figure 2: Current De-rating

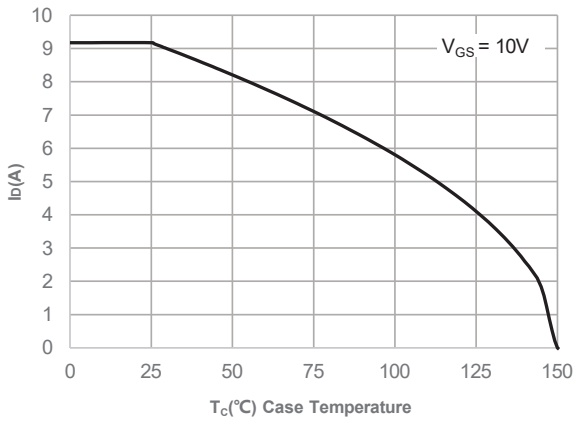


Figure 3: Normalized Maximum Transient Thermal Impedance

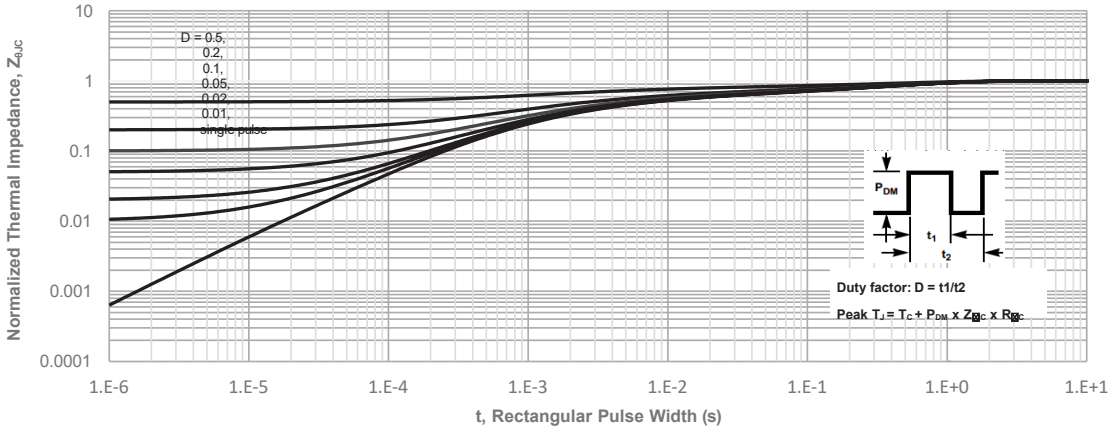
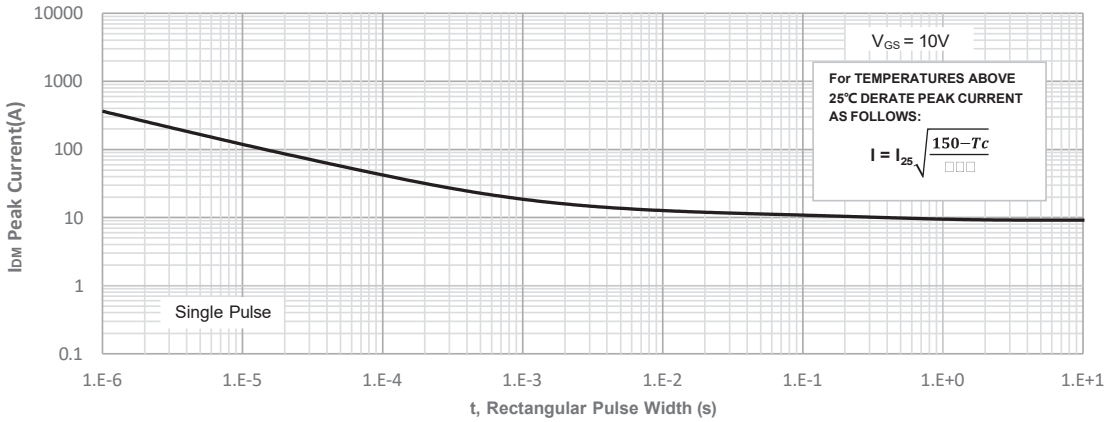


Figure 4: Peak Current Capacity



Typical Performance Characteristics

Figure 5: Output Characteristics

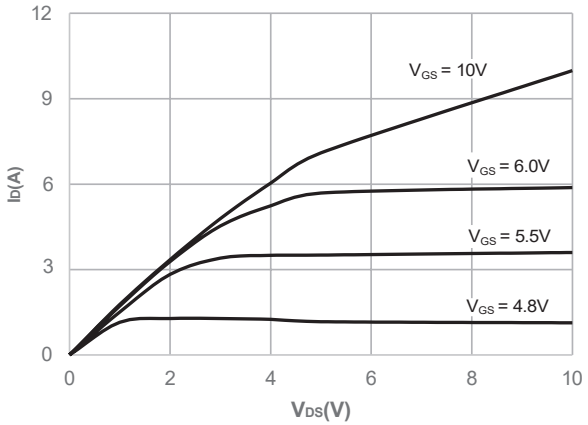


Figure 6: Typical Transfer Characteristics

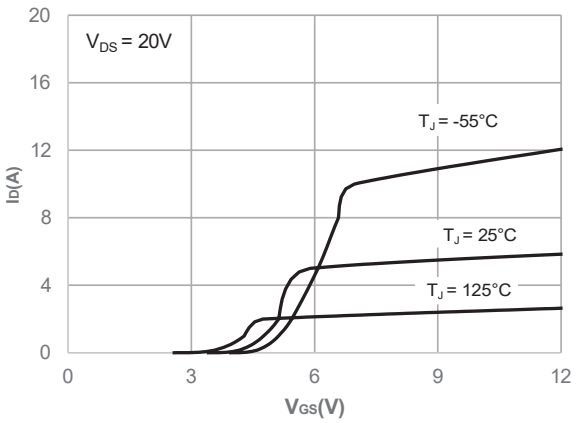


Figure 7: On-resistance vs. Drain Current

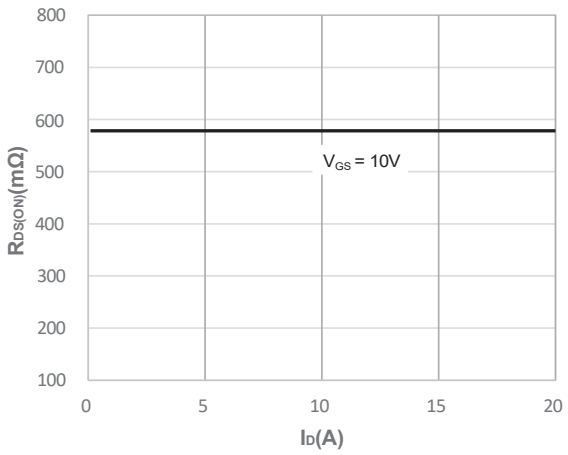


Figure 8: Body Diode Characteristics

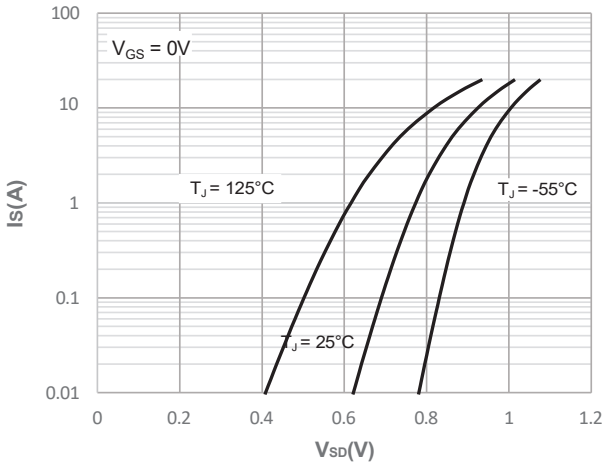


Figure 9: Gate Charge Characteristics

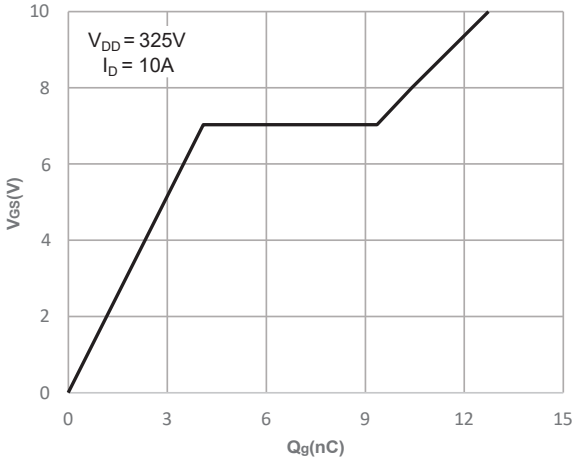
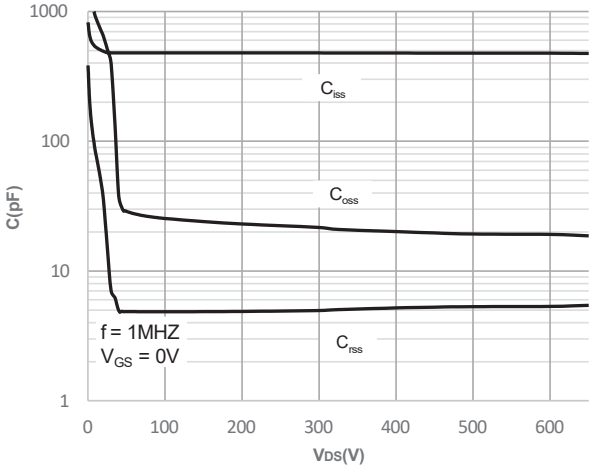


Figure 10: Capacitance Characteristics



Typical Performance Characteristics

Figure 11: Normalized Breakdown voltage vs. Junction Temperature

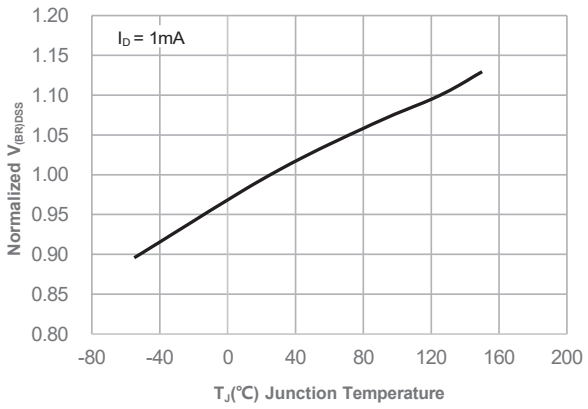


Figure 12: Normalized on Resistance vs. Junction Temperature

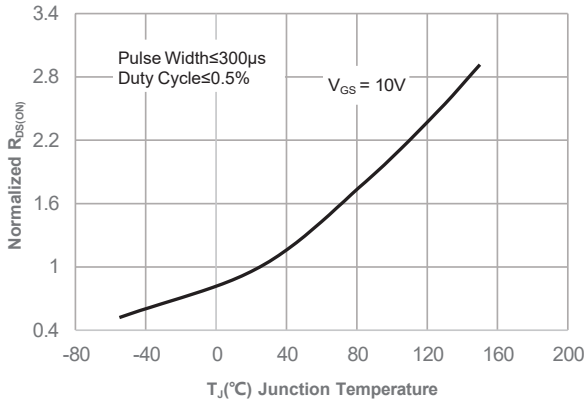


Figure 13: Normalized Threshold Voltage vs. Junction Temperature

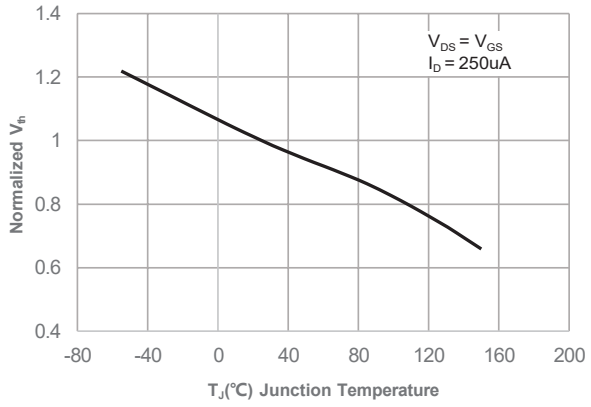


Figure 14: $R_{DS(ON)}$ vs. V_{GS}

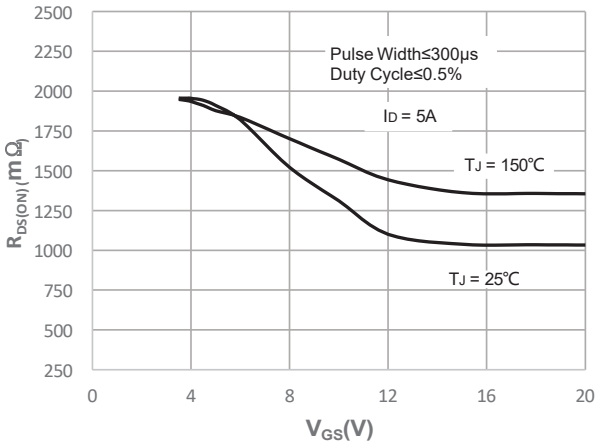
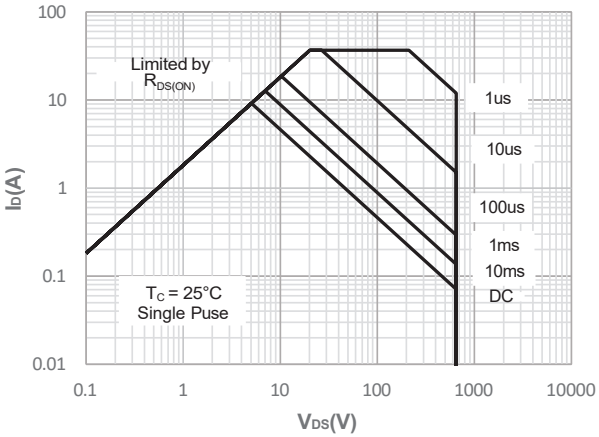


Figure 15: Maximum Safe Operating Area



Test Circuit

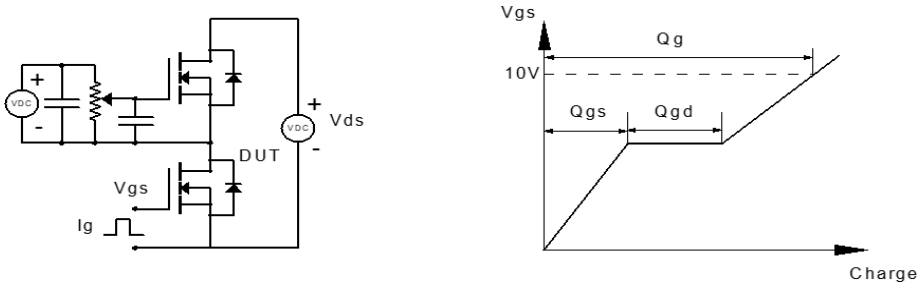


Figure 1: Gate Charge Test Circuit & Waveform

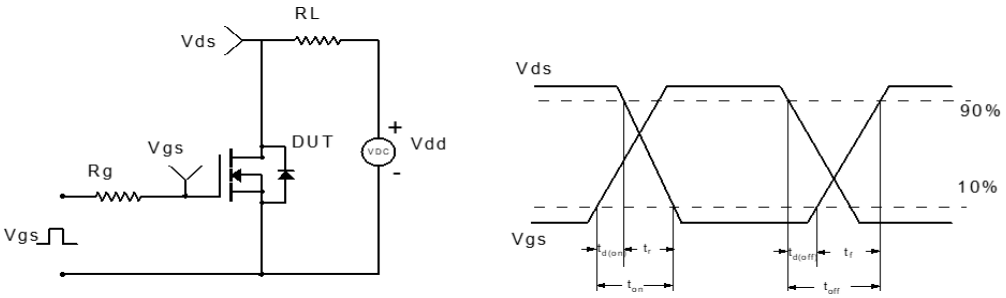


Figure 2: Resistive Switching Test Circuit & Waveform

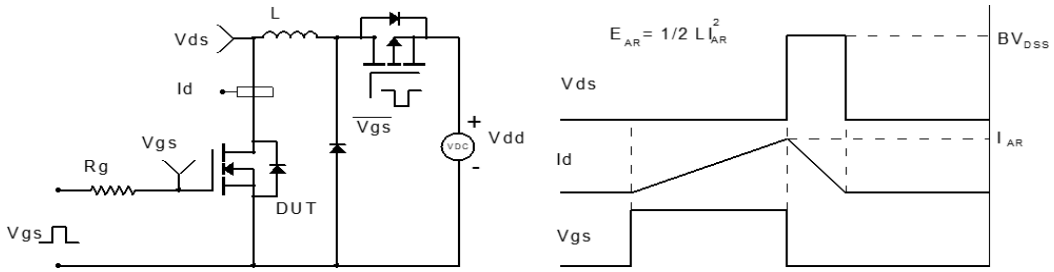


Figure 3: Unclamped Inductive Switching Test Circuit& Waveform

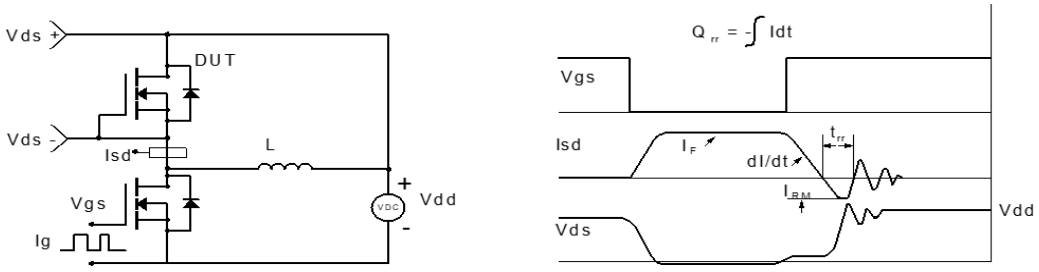


Figure 4: Diode Recovery Test Circuit & Waveform