

Features

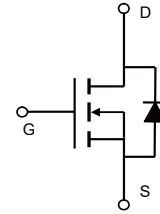
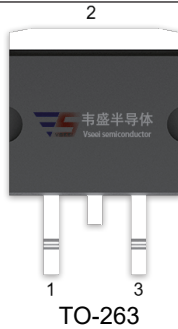
- Excellent $R_{DS(ON)}$ and Low Gate Charge
- 100% UIS Tested
- 100% ΔV_{ds} Tested
- Halogen-free; RoHS-compliant

Applications

- SMPS with PFC
- Flyback and LLC topologies
- Silver ATX, adapter, TV, lighting, Telecom

Product Summary

Parameters	Value	Unit
V_{DSS}	650	V
$V_{GS(th)}_{Typ}$	3.3	V
$I_D(@V_{GS}=10V)$	17	A
$R_{DS(ON)}_{Typ}(@V_{GS}=10V)$	156	m Ω



Schematic

Ordering Information

Device	Marking	MSL	Form	Package	Reel(pcs)	Per Carton (pcs)
VSM17N65-T3	VSM17N65	3	Tape&Reel	TO-263	800	4000

Absolute Maximum Ratings (@ $T_C = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Value	Unit
V_{DS}	Drain-to-Source Voltage	650	V
V_{GS}	Gate-to-Source Voltage	± 30	V
I_D	Continuous Drain Current	$T_C = 25^\circ\text{C}$ $T_C = 100^\circ\text{C}$	A
I_{DM}	Pulsed Drain Current ⁽¹⁾	Refer to Fig.4	A
E_{AS}	Single Pulsed Avalanche Energy ⁽²⁾	65	mJ
P_D	Power Dissipation	$T_C = 25^\circ\text{C}$ $T_C = 100^\circ\text{C}$	W
T_J, T_{STG}	Junction & Storage Temperature Range	-55 to 150	$^\circ\text{C}$

Thermal Characteristics

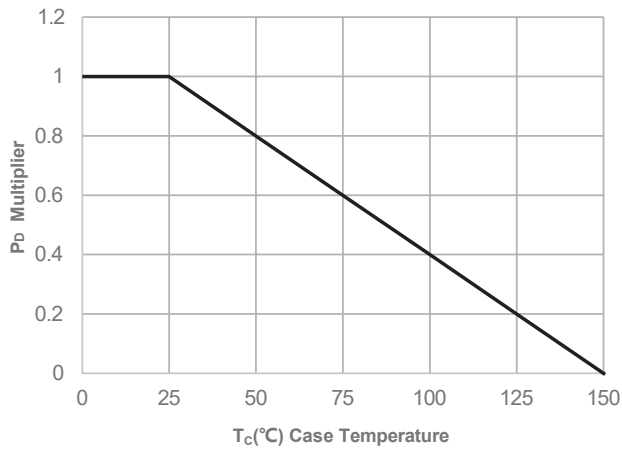
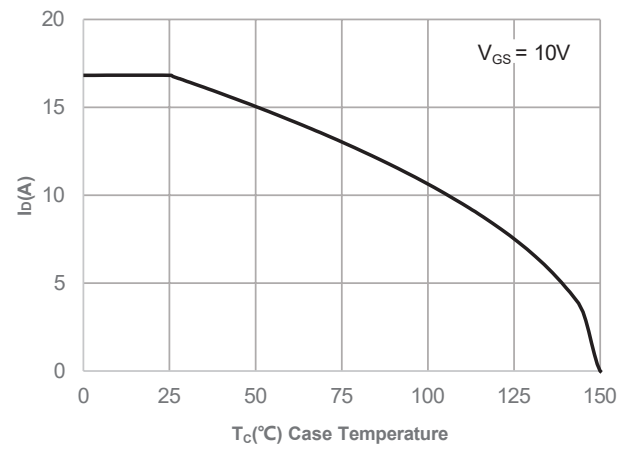
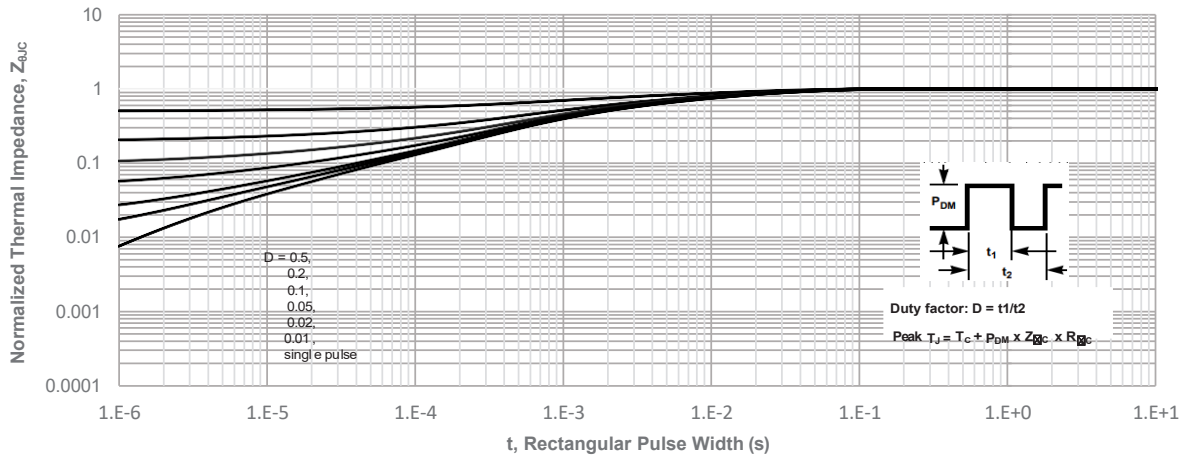
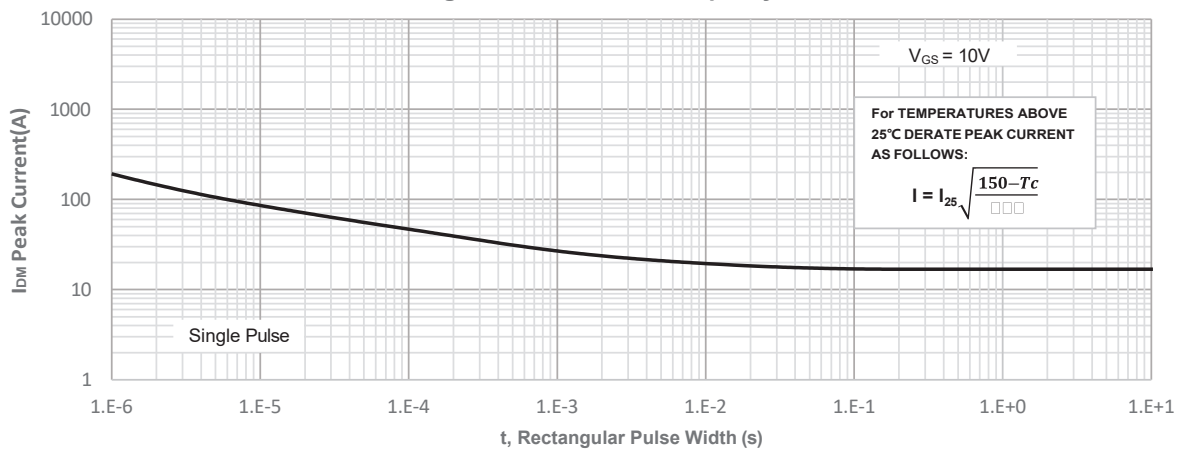
Symbol	Parameter	Max	Unit
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient ⁽³⁾	33	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance, Junction to Case	0.9	

Electrical Characteristics ($T_J = 25^{\circ}\text{C}$ unless otherwise specified)

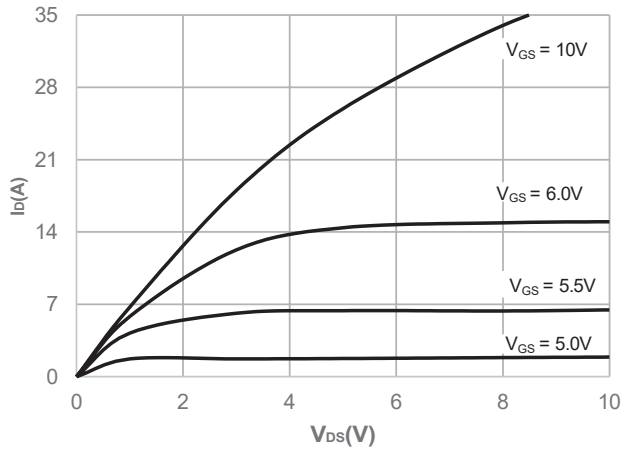
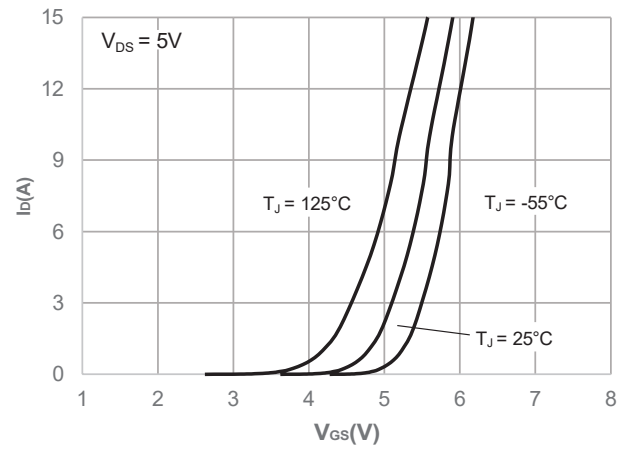
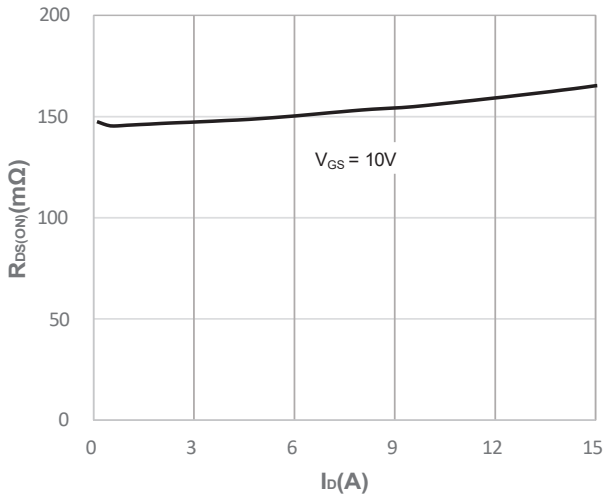
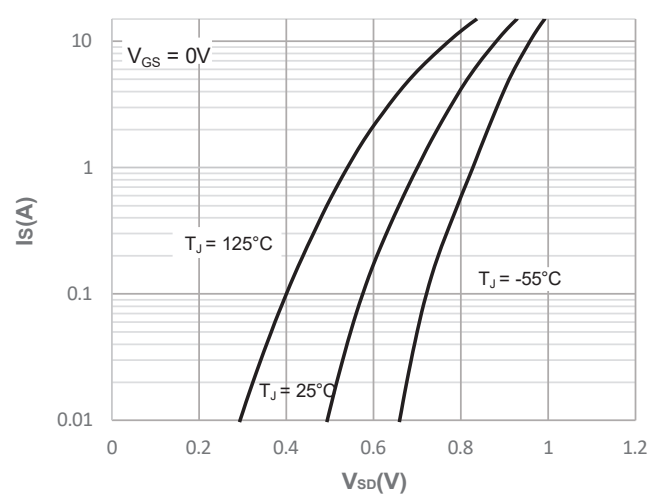
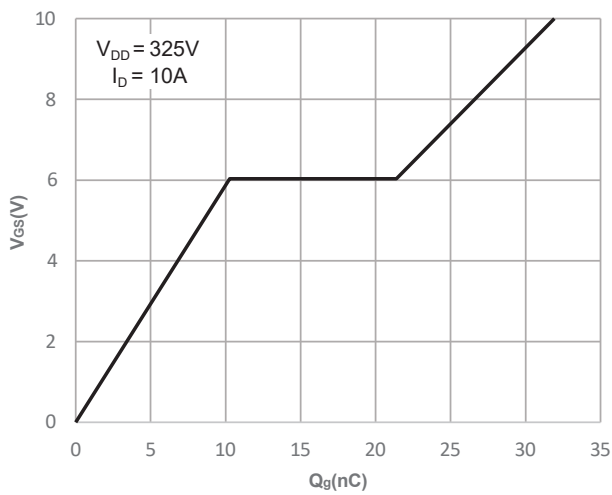
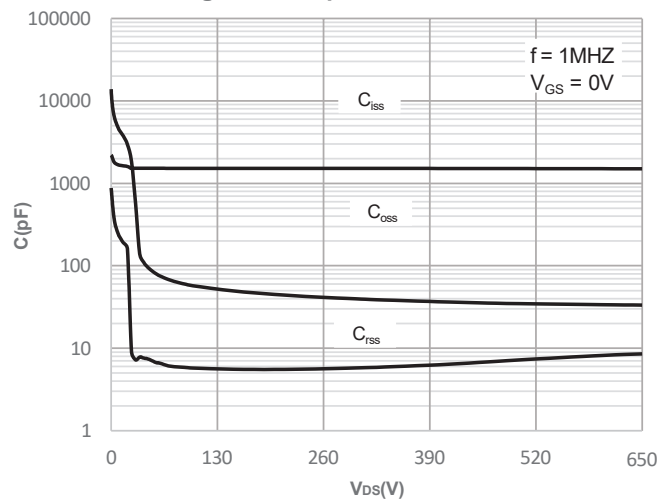
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0V	650	-	-	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 650V, V _{GS} = 0V	-	-	10.0	μA
I _{GSS}	Gate-Body Leakage Current	V _{DS} = 0V, V _{GS} = ±30V	-	-	±100	nA
On Characteristics						
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250 μA	2.3	3.3	4.3	V
R _{DS(ON)}	Static Drain-Source ON-Resistance ⁽⁴⁾	V _{GS} = 10V, I _D = 10A	-	156	190	mΩ
Dynamic Characteristics						
R _g	Gate Resistance	f = 1MHz	-	4.9	-	Ω
C _{iss}	Input Capacitance	V _{GS} = 0V, V _{DS} = 325V, f = 1MHz	1084	1517	2276	pF
C _{oss}	Output Capacitance		28	39	58	pF
C _{rss}	Reverse Transfer Capacitance		-	5.9	-	pF
Q _g	Total Gate Charge	V _{GS} = 0 to 10V V _{DS} = 325V, I _D = 10A	23	32	48	nC
Q _{gs}	Gate Source Charge		-	10	-	nC
Q _{gd}	Gate Drain("Miller") Charge		-	11	-	nC
Switching Characteristics						
t _{d(on)}	Turn-On DelayTime	V _{GS} = 10V, V _{DD} = 310V I _D = 10A, R _{GEN} = 24 Ω	-	36	-	ns
t _r	Turn-On Rise Time		-	38	-	ns
t _{d(off)}	Turn-Off DelayTime		-	100	-	ns
t _f	Turn-Off Fall Time		-	30	-	ns
Body Diode Characteristics						
I _S	Maximum Continuous Body Diode Forward Current		-	-	17	A
I _{SM}	Maximum Pulsed Body Diode Forward Current		-	-	67	A
V _{SD}	Body Diode Forward Voltage	V _{GS} = 0V, I _S = 10A	-		1.2	V
trr	Body Diode Reverse Recovery Time	I _F = 10A, di/dt = 100A/us	94	131	197	ns
Qrr	Body Diode Reverse Recovery Charge		-	851	-	nC

- Notes:
1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature.
 2. E_{AS} condition: Starting $T_J = 25^{\circ}\text{C}$, $V_{DD} = 50\text{V}$, $V_{GS} = 10\text{V}$, $R_G = 25\text{ohm}$, $L = 10\text{mH}$, $I_{AS} = 3.6\text{A}$, $V_{DD} = 0\text{V}$ during time in avalanche.
 3. $R_{\theta JA}$ is measured with the device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square pad layout.
 4. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 0.5\%$.

Typical Performance Characteristics

Figure 1: Power De-rating

Figure 2: Current De-rating

Figure 3: Normalized Maximum Transient Thermal Impedance

Figure 4: Peak Current Capacity


Typical Performance Characteristics

Figure 5: Output Characteristics

Figure 6: Typical Transfer Characteristics

Figure 7: On-resistance vs. Drain Current

Figure 8: Body Diode Characteristics

Figure 9: Gate Charge Characteristics

Figure 10: Capacitance Characteristics


Typical Performance Characteristics

Figure 11: Normalized Breakdown voltage vs. Junction Temperature

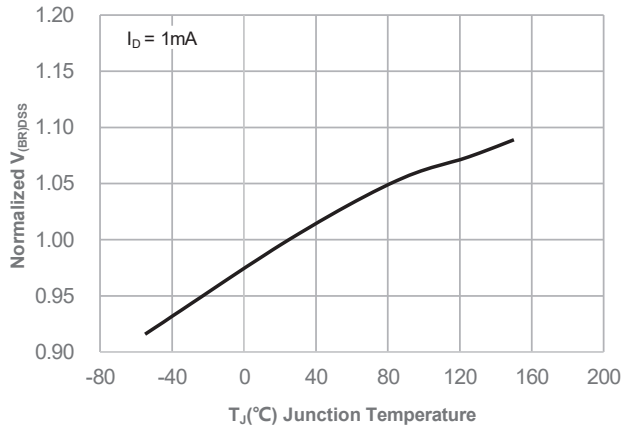


Figure 12: Normalized on Resistance vs. Junction Temperature

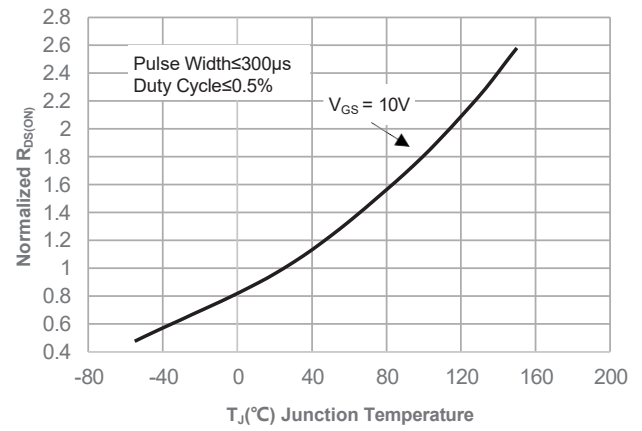


Figure 13: Normalized Threshold Voltage vs. Junction Temperature

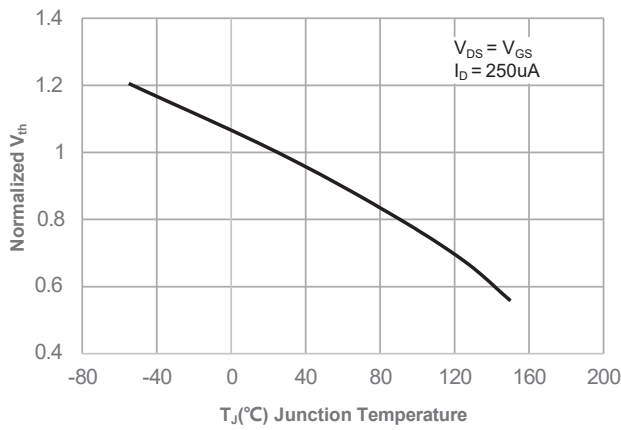


Figure 14: RDS(ON) vs. VGS

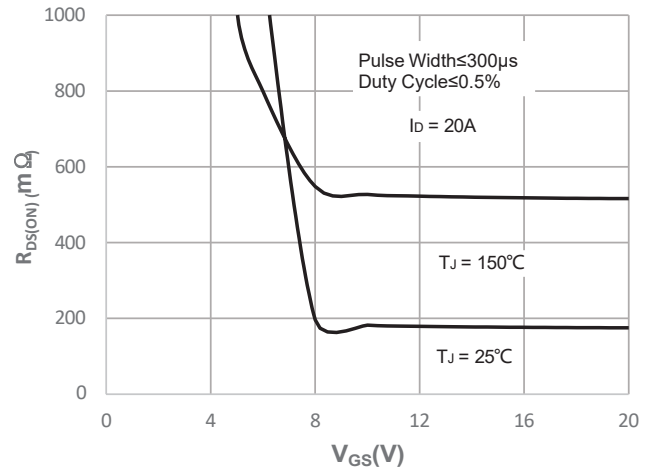
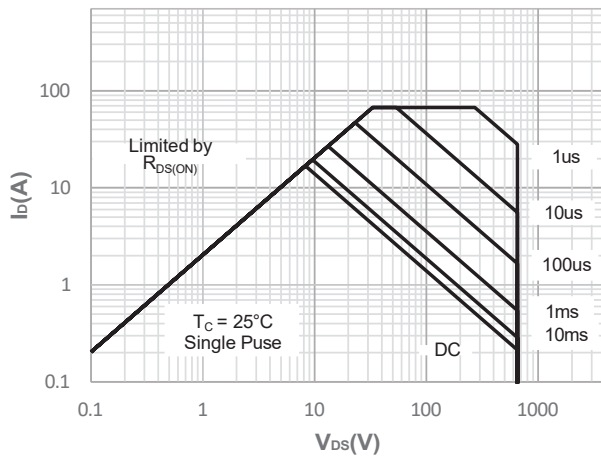


Figure 15: Maximum Safe Operating Area



Test Circuit



Figure 1: Gate Charge Test Circuit & Waveform



Figure 2: Resistive Switching Test Circuit & Waveform



Figure 3: Unclamped Inductive Switching Test Circuit & Waveform



Figure 4: Diode Recovery Test Circuit & Waveform