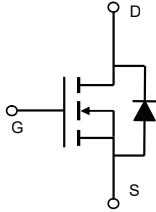


Description

Features 20V, 60A $R_{DS(ON)} < 3.9m\Omega @ V_{GS} = 4.5V$ $R_{DS(ON)} < 4.9m\Omega @ V_{GS} = 2.5V$ - Advanced Trench Technology - Excellent $R_{DS(ON)}$ and Low Gate Charge - Lead Free	Applications - Load Switch - PWM Application - Power Management <i>100% UIS TESTED!</i> <i>100% ΔV_{ds} TESTED!</i>
 DFN3x3	 Schematic

Package Marking and Ordering Information

Device Marking	Device	Outline	Package	Reel Size	Reel(pcs)	Per Carton (pcs)
VSM60N02	VSM60N02-D33	TAPING	DFN3x3	13"	5000	50000

Absolute Maximum Ratings (@ $T_C = 25^\circ\text{C}$ unless otherwise specified)

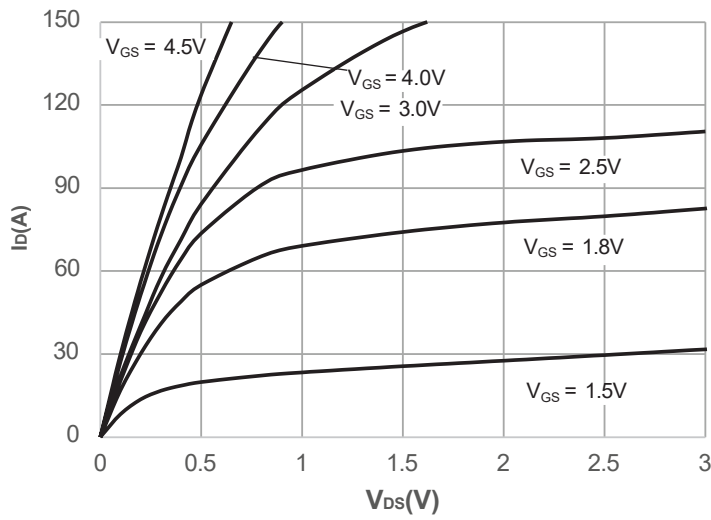
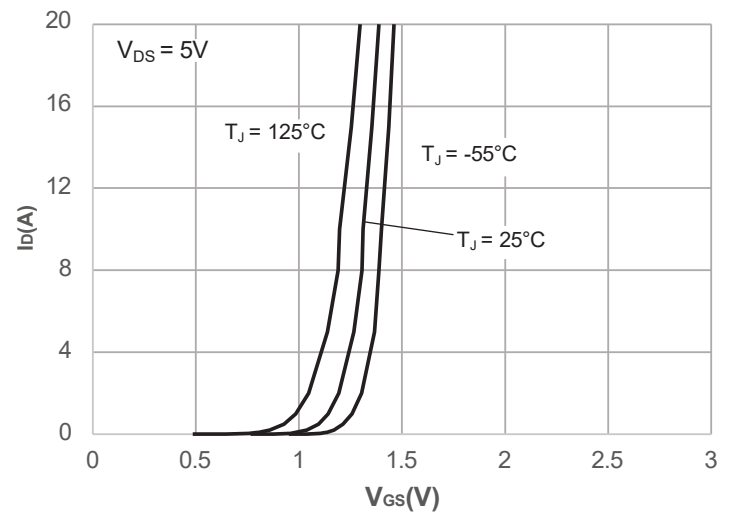
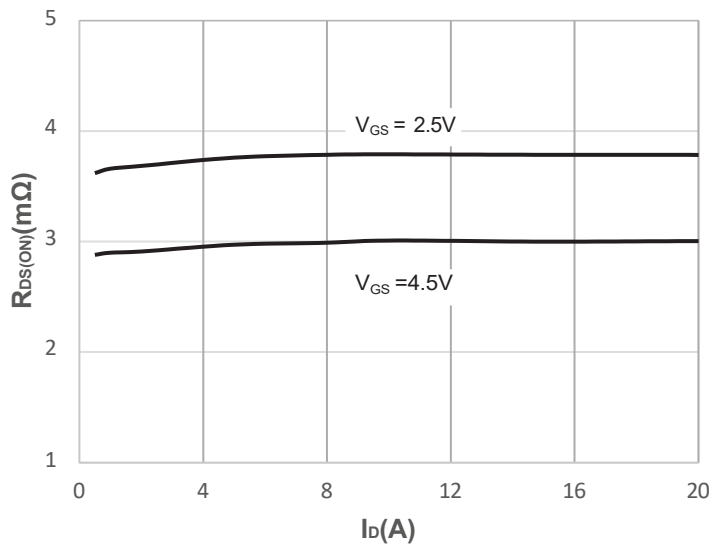
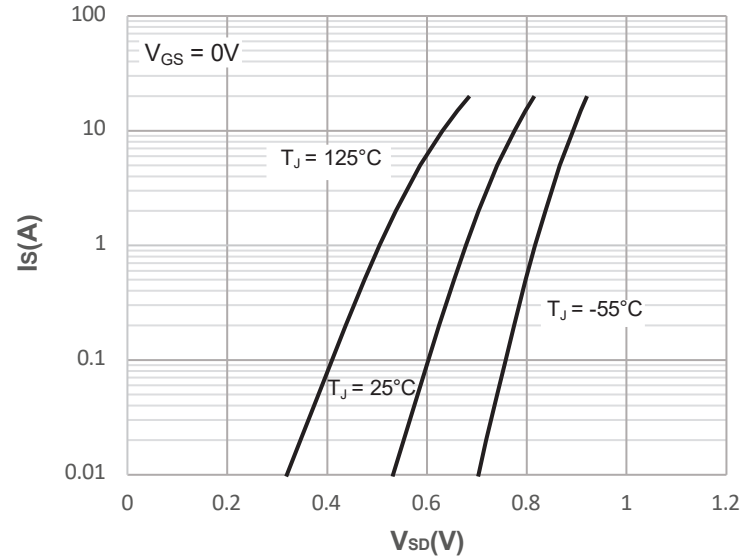
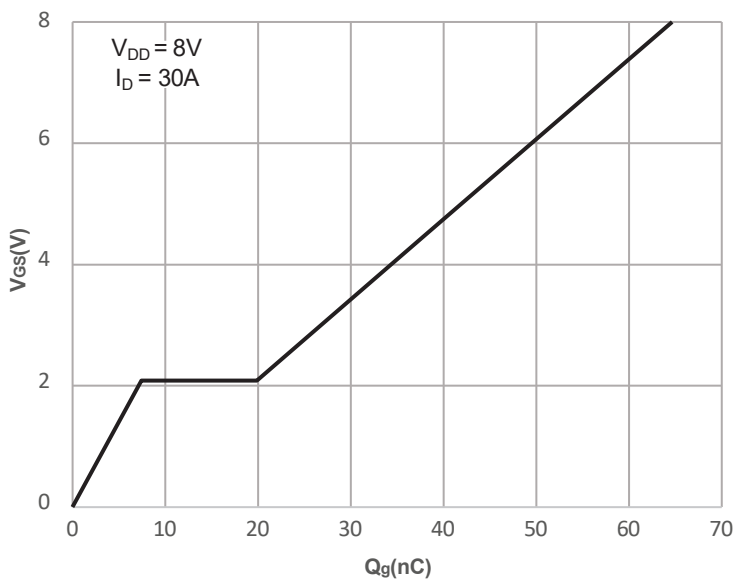
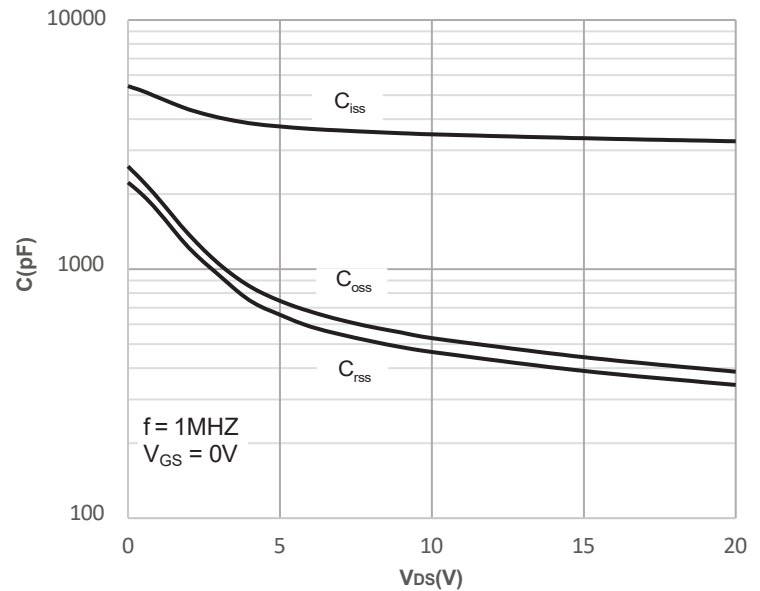
Symbol	Parameter	Value	Units
V_{DS}	Drain-to-Source Voltage	20	V
V_{GS}	Gate-to-Source Voltage	± 12	V
I_D	Continuous Drain Current	$T_C = 25^\circ\text{C}$	A
		$T_C = 100^\circ\text{C}$	
I_{DM}	Pulsed Drain Current ⁽¹⁾	240	A
E_{AS}	Single Pulsed Avalanche Energy ⁽²⁾	121	mJ
P_D	Power Dissipation	$T_C = 25^\circ\text{C}$	W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient ⁽³⁾	40	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance, Junction to Case	3.2	
T_J, T_{STG}	Junction & Storage Temperature Range	-55 to 150	$^\circ\text{C}$

Electrical Characteristics ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0V	20	-	-	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 20V, V _{GS} = 0V	-	-	1.0	μA
I _{GSS}	Gate-Body Leakage Current	V _{DS} = 0V, V _{GS} = ±12V	-	-	±100	nA
On Characteristics						
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250 μA	0.5	0.8	1.0	V
R _{DS(ON)}	Static Drain-Source ON-Resistance ⁽⁴⁾	V _{GS} =4.5V, I _D =30A	-	3.0	3.9	mΩ
		V _{GS} = 2.5V, I _D =20A	-	3.8	4.9	mΩ
Dynamic Characteristics						
C _{iss}	Input Capacitance	V _{GS} = 0V, V _{DS} = 10V, f = 1MHz	-	3476	-	pF
C _{oss}	Output Capacitance		-	528	-	pF
C _{rss}	Reverse Transfer Capacitance		-	464	-	pF
Q _g	Total Gate Charge	V _{GS} = 0 to 8V V _{DS} = 10V, I _D = 30A	-	65	-	nC
Q _{gs}	Gate Source Charge		-	8	-	nC
Q _{gd}	Gate Drain("Miller") Charge		-	12	-	nC
Switching Characteristics						
t _{d(on)}	Turn-On DelayTime	V _{GS} = 10V, V _{DD} = 10V I _D = 30A, R _{GEN} = 3 Ω	-	8	-	ns
t _r	Turn-On Rise Time		-	19	-	ns
t _{d(off)}	Turn-Off DelayTime		-	73	-	ns
t _f	Turn-Off Fall Time		-	80	-	ns
Drain-Source Diode Characteristics and Max Ratings						
I _S	Maximum Continuous Drain to Source Diode Forward Current		-	-	60	A
I _{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	240	A
V _{SD}	Drain to Source Diode Forward Voltage	V _{GS} = 0V, I _S = 30A	-	-	1.2	V
t _{rr}	Body Diode Reverse Recovery Time	I _F = 20A, di/dt = 100A/us	-	16	-	ns
Q _{rr}	Body Diode Reverse Recovery Charge		-	5.6	-	nC

- Notes:
1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature.
 2. E_{AS} condition: Starting $T_J = 25^\circ\text{C}$, $V_{DD} = 10\text{V}$, $V_G = 10\text{V}$, $R_G = 25\text{ohm}$, $L = 0.5\text{mH}$, $I_{AS} = 22\text{A}$
 3. $R_{\theta JA}$ is measured with the device mounted on a 1inch² pad of 2oz copper FR4 PCB
 4. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 0.5\%$.

Typical Performance Characteristics

Figure 1: Output Characteristics

Figure 2: Typical Transfer Characteristics

Figure 3: On-resistance vs. Drain Current

Figure 4: Body Diode Characteristics

Figure 5: Gate Charge Characteristics

Figure 6: Capacitance Characteristics


Typical Performance Characteristics

Figure 7: Normalized Breakdown voltage vs. Junction Temperature

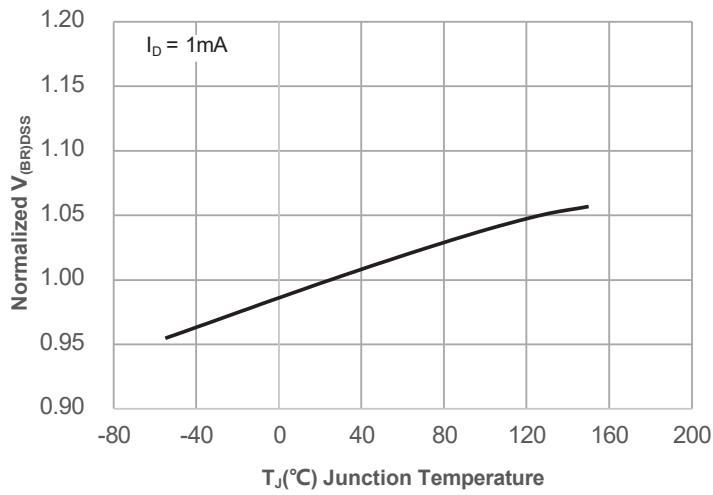


Figure 8: Normalized on Resistance vs. Junction Temperature

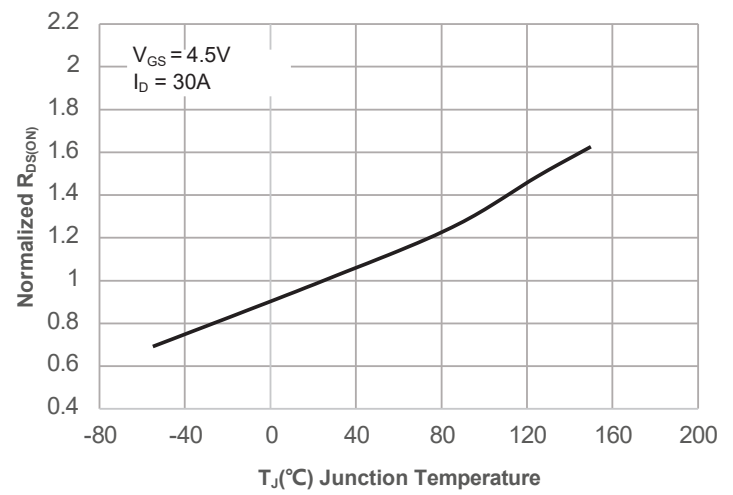


Figure 9: Maximum Safe Operating Area

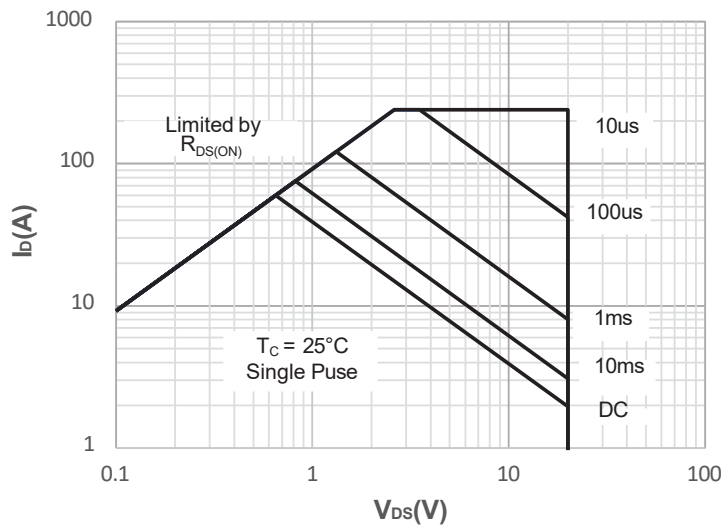


Figure 10: Maximum Continuous Driant Current vs. Case Temperature

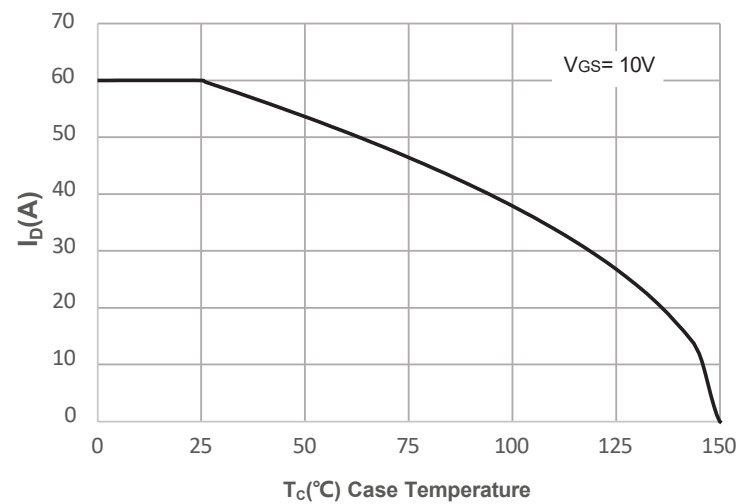


Figure 11: Normalized Maximum Transient Thermal Impedance

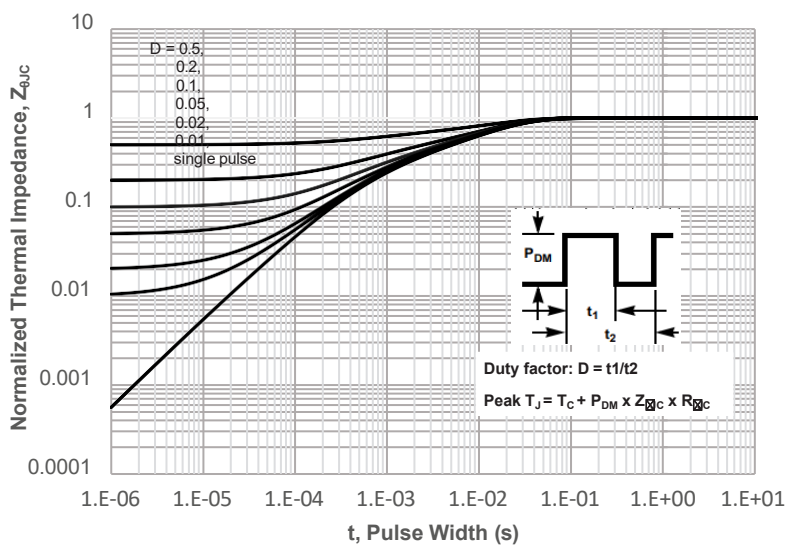
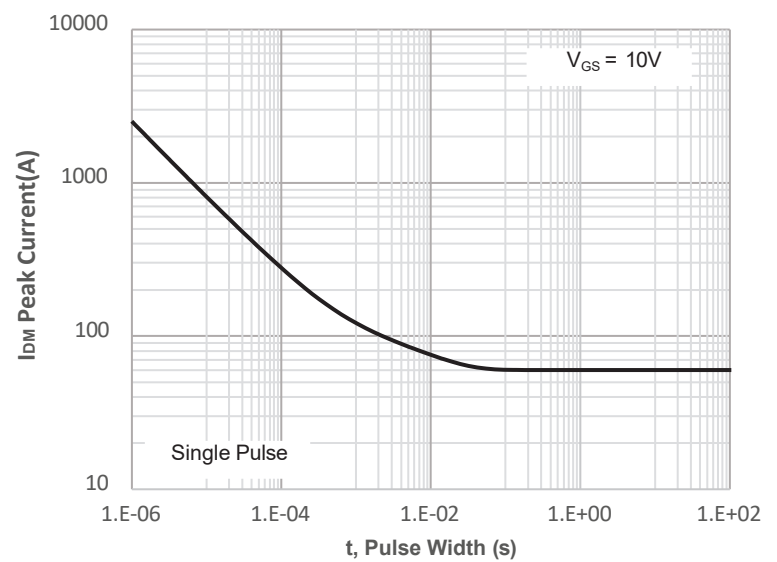


Figure 12: Peak Current Capacity



Test Circuit

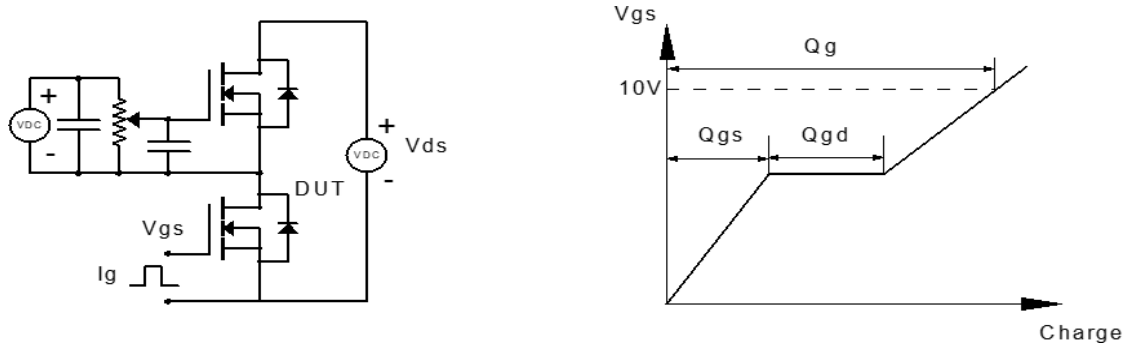


Figure 1: Gate Charge Test Circuit & Waveform

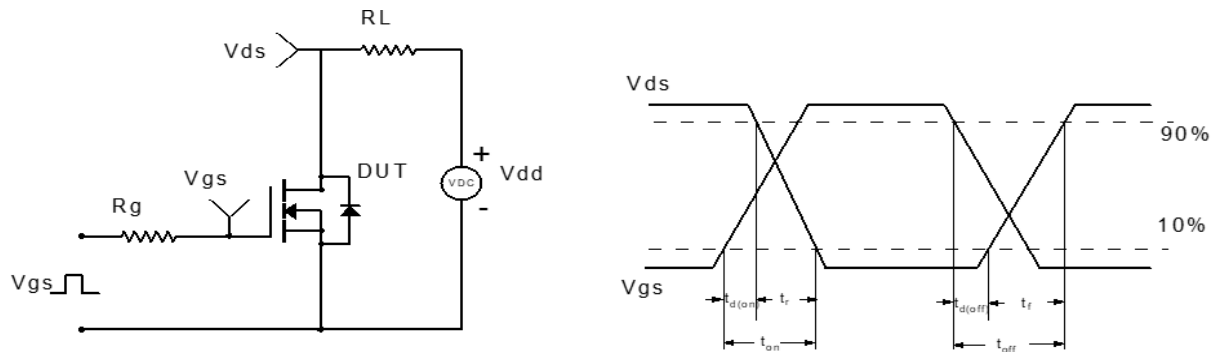


Figure 2: Resistive Switching Test Circuit & Waveform

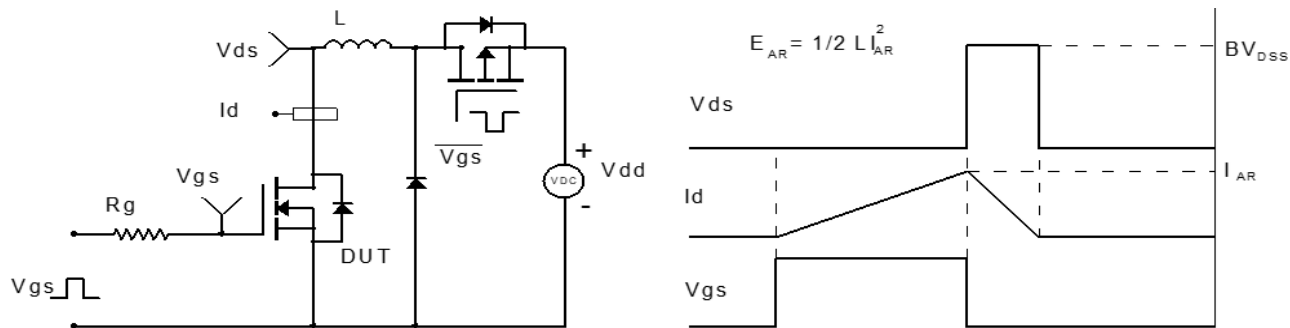


Figure 3: Unclamped Inductive Switching Test Circuit& Waveform

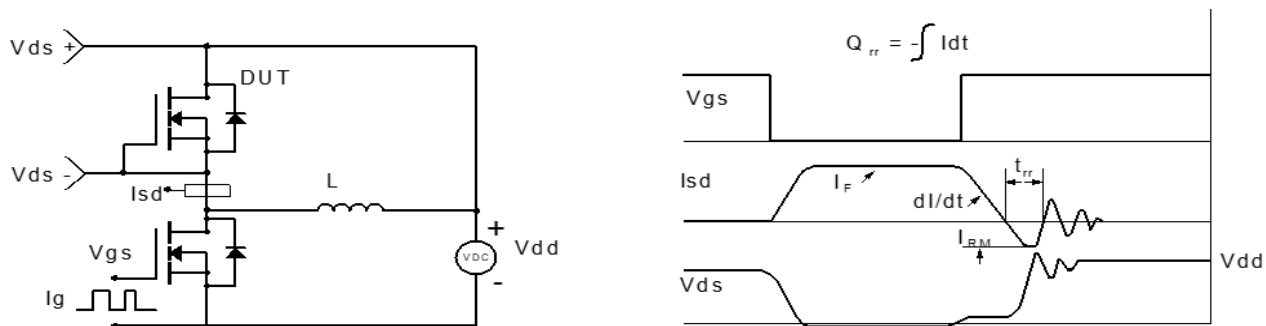


Figure 4: Diode Recovery Test Circuit & Waveform