

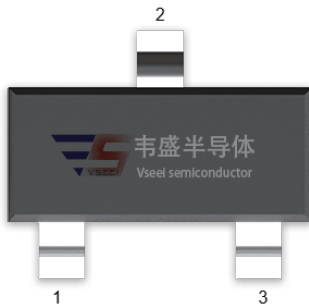
Description

Features

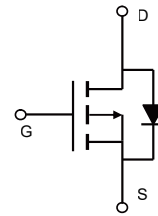
- -30V, -4.2A
 $R_{DS(ON)} < 47m\Omega @ V_{GS} = -10V$
 $R_{DS(ON)} < 53m\Omega @ V_{GS} = -4.5V$
 $R_{DS(ON)} < 68m\Omega @ V_{GS} = -2.5V$
- Advanced Trench Technology
- Excellent $R_{DS(ON)}$ and Low Gate Charge
- Lead Free

Applications

- Load Switch
- PWM Application
- Power Management



SOT-23



Schematic

Package Marking and Ordering Information

Device Marking	Device	Outline	Package	Reel Size	Reel(pcs)	Per Carton (pcs)
VSM3401A	VSM3401A-S2	TAPING	SOT-23	7"	3000	120000

Absolute Maximum Ratings (@ $T_A = 25^\circ\text{C}$ unless otherwise specified)

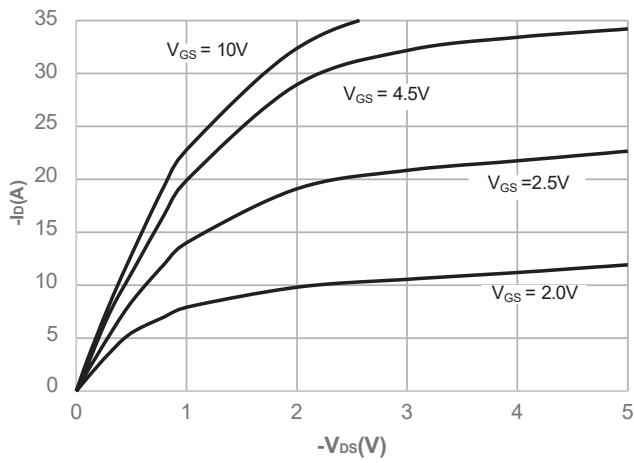
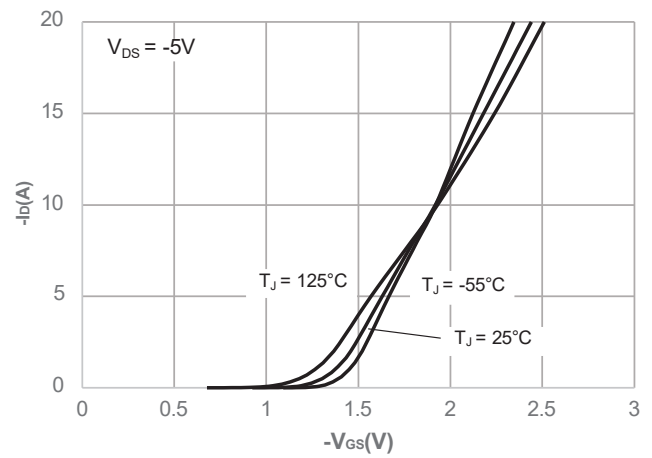
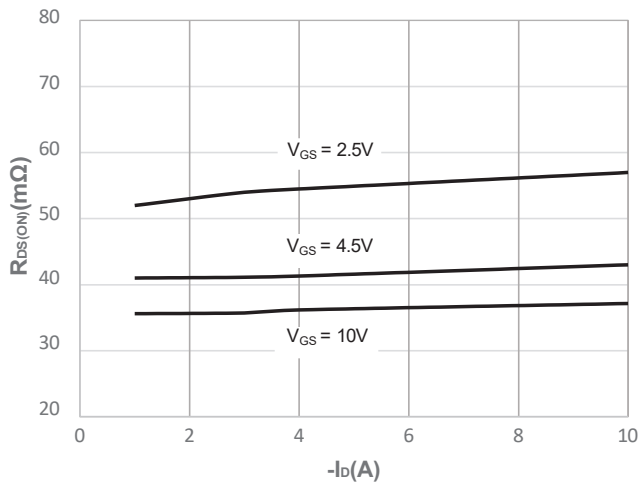
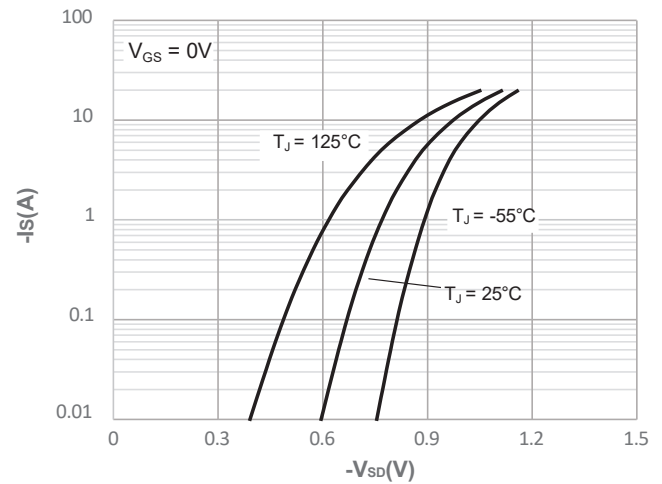
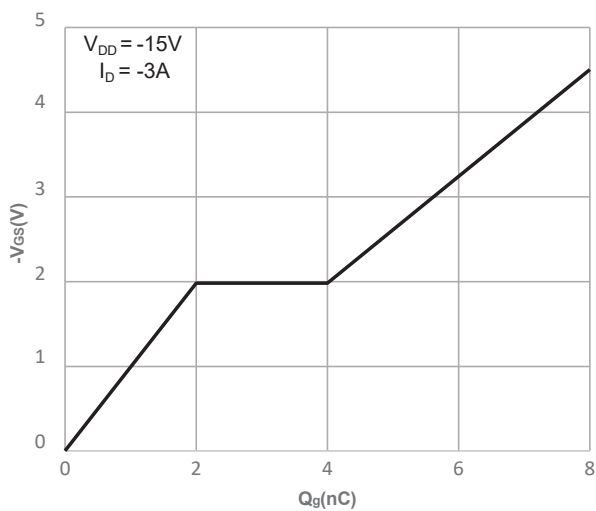
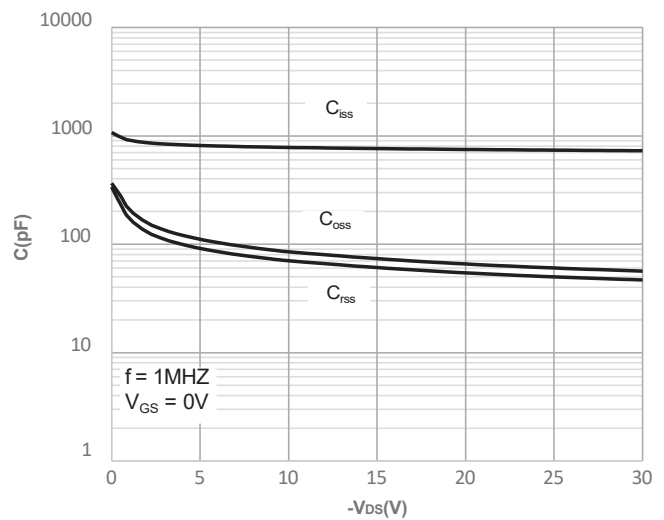
Symbol	Parameter	Value	Units
V_{DS}	Drain-to-Source Voltage	-30	V
V_{GS}	Gate-to-Source Voltage	± 12	V
I_D	Continuous Drain Current	$T_A = 25^\circ\text{C}$	A
		$T_A = 100^\circ\text{C}$	
I_{DM}	Pulsed Drain Current ⁽¹⁾	-17	A
P_D	Power Dissipation	$T_A = 25^\circ\text{C}$	W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient ⁽²⁾	108	$^\circ\text{C/W}$
T_J, T_{STG}	Junction & Storage Temperature Range	-55 to 150	$^\circ\text{C}$

Electrical Characteristics ($T_J = 25^{\circ}\text{C}$ unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	I _D = -250 μA, V _{GS} = 0V	-30	-	-	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = -30V, V _{GS} = 0V	-	-	1.0	μA
I _{GSS}	Gate-Body Leakage Current	V _{DS} = 0V, V _{GS} = ±12V	-	-	±100	nA
On Characteristics						
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = -250 μA	-0.6	-0.9	-1.3	V
R _{DS(ON)}	Static Drain-Source ON-Resistance ⁽³⁾	V _{GS} = -10V, I _D = -4A	-	36	47	mΩ
		V _{GS} = -4.5V, I _D = -3A	-	41	53	mΩ
		V _{GS} = -2.5V, I _D = -1A	-	52	68	mΩ
Dynamic Characteristics						
C _{iss}	Input Capacitance	V _{GS} = 0V, V _{DS} = -15V, f = 1MHz	-	762	-	pF
C _{oss}	Output Capacitance		-	74	-	pF
C _{rss}	Reverse Transfer Capacitance		-	61	-	pF
Q _g	Total Gate Charge	V _{GS} = 0 to -4.5V V _{DS} = -15V, I _D = -3A	-	8	-	nC
Q _{gs}	Gate Source Charge		-	2	-	nC
Q _{gd}	Gate Drain("Miller") Charge		-	2	-	nC
Switching Characteristics						
t _{d(on)}	Turn-On DelayTime	V _{GS} = -4.5V, V _{DD} = -15V I _D = -3A, R _{GEN} = 3 Ω	-	8	-	ns
t _r	Turn-On Rise Time		-	16	-	ns
t _{d(off)}	Turn-Off DelayTime		-	46	-	ns
t _f	Turn-Off Fall Time		-	34	-	ns
Drain-Source Diode Characteristics and Max Ratings						
I _S	Maximum Continuous Drain to Source Diode Forward Current		-	-	-4.2	A
I _{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	-17	A
V _{SD}	Drain to Source Diode Forward Voltage	V _{GS} = 0V, I _S = -4.2A	-	-	-1.2	V
trr	Body Diode Reverse Recovery Time	I _F = -3A, di/dt = 100A/us	-	8	-	ns
Qrr	Body Diode Reverse Recovery Charge		-	3	-	nC

- Notes:
1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature.
 2. $R_{\theta JA}$ is measured with the device mounted on a 1inch² pad of 2oz copper FR4 PCB
 3. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 0.5\%$.

Typical Performance Characteristics

Figure 1: Output Characteristics

Figure 2: Typical Transfer Characteristics

Figure 3: On-resistance vs. Drain Current

Figure 4: Body Diode Characteristics

Figure 5: Gate Charge Characteristics

Figure 6: Capacitance Characteristics


Typical Performance Characteristics

Figure 7: Normalized Breakdown voltage vs. Junction Temperature

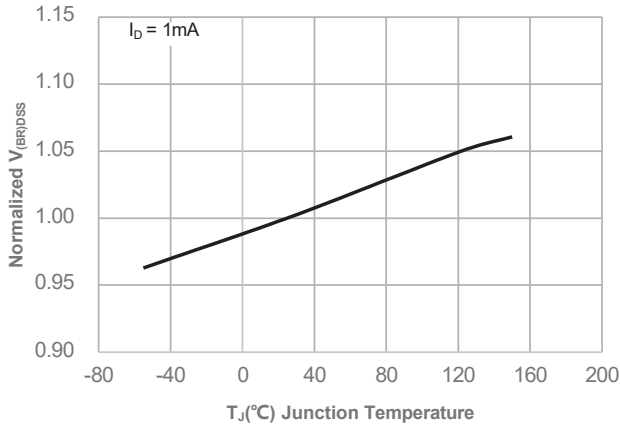


Figure 8: Normalized on Resistance vs. Junction Temperature

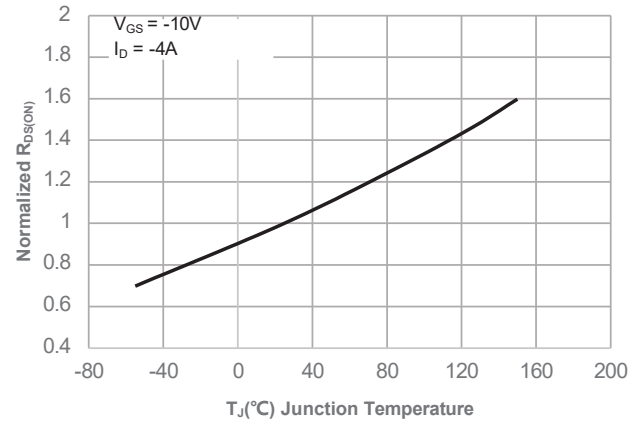


Figure 9: Maximum Safe Operating Area

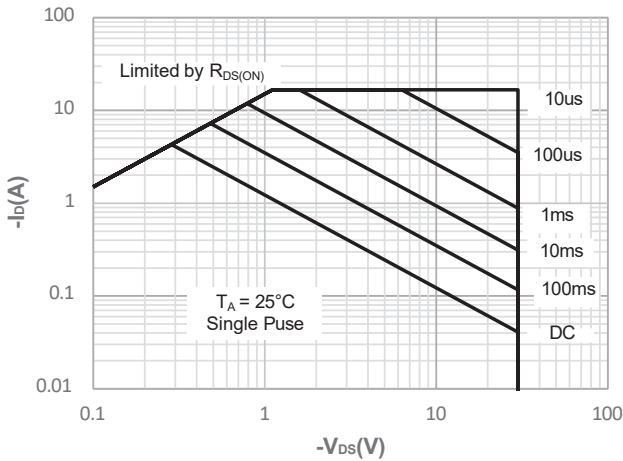


Figure 10: Maximum Continuous Driand Current vs. Ambient Temperature

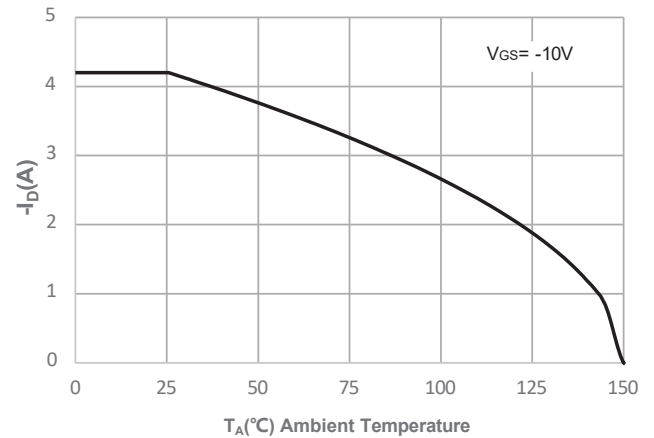


Figure 11: Normalized Maximum Transient Thermal Impedance

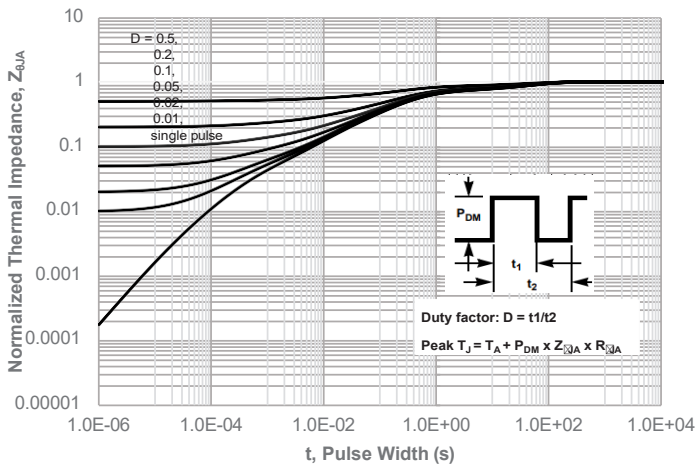
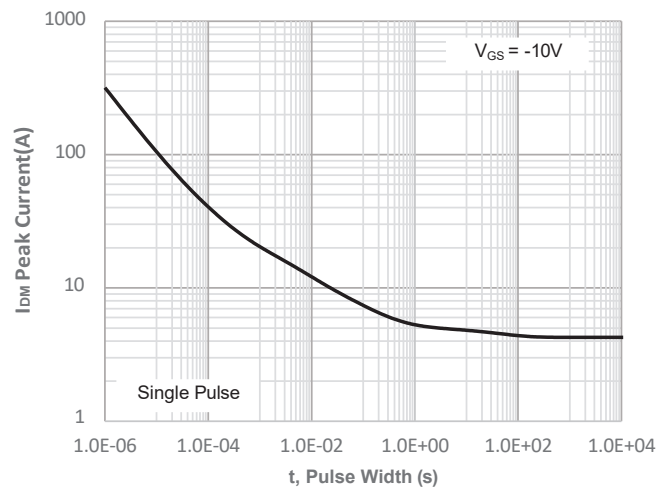


Figure 12: Peak Current Capacity



Test Circuit

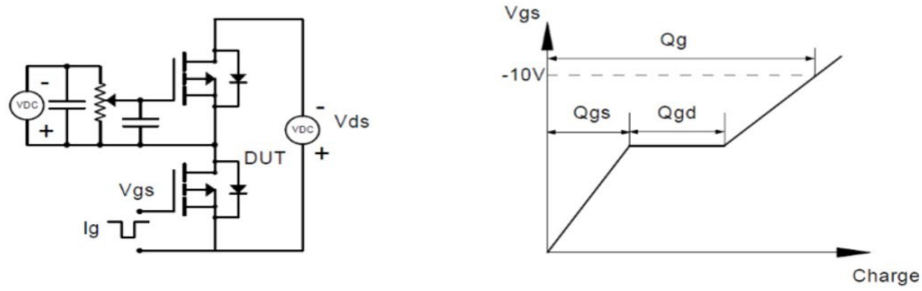


Figure 1: Gate Charge Test Circuit & Waveform

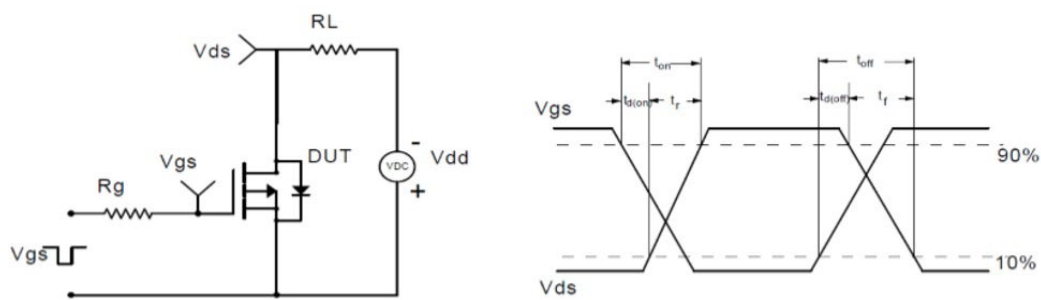


Figure 2: Resistive Switching Test Circuit & Waveform

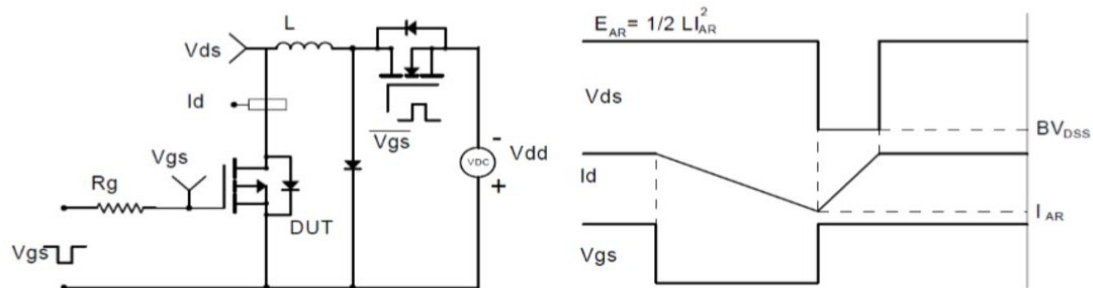


Figure 3: Unclamped Inductive Switching Test Circuit & Waveform

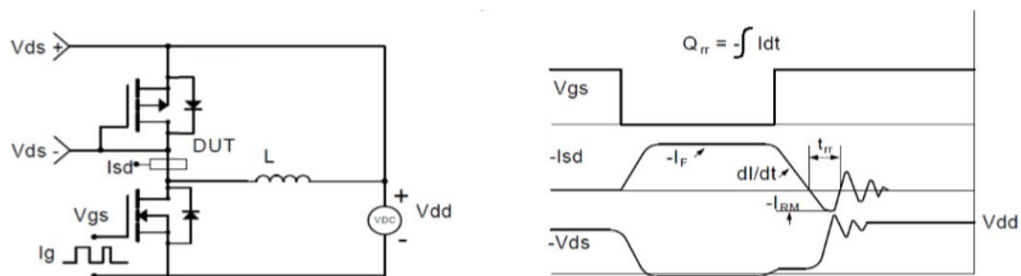


Figure 4: Diode Recovery Test Circuit & Waveform