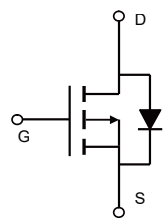
Features

- Excellent $R_{DS(ON)}$ and Low Gate Charge
- 100% UIS Tested
- 100% ΔVds Tested
- Halogen-free; RoHS-compliant
- **Applications**
- Load Switch
- PWM Application
- Power Management

Product Summary

Parameters	Value	Unit
V_{DSS}	-30	V
$V_{GS(th)\_Typ}$	-1.6	V
I_D(@V_{GS}=-10V)	-55	A
$R_{DS(ON)\_Typ}$(@V_{GS}=-10V	6.1	mΩ
$R_{DS(ON)\_Typ}$(@V_{GS}=-4.5V	8.9	mΩ

TO-252



Schematic

Ordering Information

Device	Marking	MSL	Form	Package	Reel(pcs)	Per Carton (pcs)
VSM55P03-T2	VSM55P03	3	Tape&Reel	TO-252	2500	25000

Absolute Maximum Ratings (@ T_C = 25°C unless otherwise specified)

Symbol	Parameter		Value	Unit
V_{DS}	Drain-to-Source Voltage		-30	V
V_{GS}	Gate-to-Source Voltage		±20	V
I_D	Continuous Drain Current	T_C = 25°C	-55	A
		T_C = 100°C	-35	
I_{DM}	Pulsed Drain Current (1)		Refer to Fig.4	A
E_{AS}	Single Pulsed Avalanche Energy (2)		206	mJ
P_D	Power Dissipation	T_C = 25°C	43	W
		T_C = 100°C	17	
T_J, T_{STG}	Junction & Storage Temperature Range		-55 to 150	°C

Thermal Characteristics

Symbol	Parameter	Max	Unit
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient(3)	41	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction to Case	2.9	

Electrical Characteristics (T_J = 25°C unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	I_D = -250 μA, V_{GS} = 0V	-30	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -30V, V_{GS} = 0V	-	-	-1.0	μA
I_{GSS}	Gate-Body Leakage Current	V_{DS} = 0V, V_{GS} = ±20V	-	-	±100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = -250 μA	-1.1	-1.6	-2.5	V
$R_{DS(ON)}$	Static Drain-Source ON-Resistance(4)	V_{GS} = -10V, I_D = -30A	-	6.1	10.0	mΩ
		V_{GS} = -4.5V, I_D = -20A	-	8.9	16.0	mΩ
Dynamic Characteristics						
R_g	Gate Resistance	f = 1MHz	-	5.6	-	Ω
C_{iss}	Input Capacitance	V_{GS} = 0V, V_{DS} = -15V, f = 1MHz	2489	3485	4705	pF
C_{oss}	Output Capacitance		283	397	536	pF
C_{rss}	Reverse Transfer Capacitance		240	336	454	pF
Q_g	Total Gate Charge	V_{GS} = 0 to -10V V_{DS} = -15V, I_D = -20A	44	62	83	nC
Q_{gs}	Gate Source Charge		7	10	13	nC
Q_{gd}	Gate Drain("Miller") Charge		9	12	16	nC
Switching Characteristics						
$t_{d(on)}$	Turn-On DelayTime	V_{GS} = -10V, V_{DD} = -15V I_D= -20A, R_{GEN} = 3Ω	-	16	-	ns
t_r	Turn-On Rise Time		-	62	-	ns
$t_{d(off)}$	Turn-Off DelayTime		-	55	-	ns
t_f	Turn-Off Fall Time		-	70	-	ns
Body Diode Characteristics						
I_S	Maximum Continuous Body Diode Forward Current		-	-	-55	A
I_{SM}	Maximum Pulsed Body Diode Forward Current		-	-	-221	A
V_{SD}	Body Diode Forward Voltage	V_{GS} = 0V, I_S = -30A	-		1.2	V
trr	Body Diode Reverse Recovery Time	I_F = -15A, di/dt = 100A/us	15	22	29	ns
Qrr	Body Diode Reverse Recovery Charge		-	11.5	-	nC

Notes:

1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature.
2. E_{AS} condition: Starting T_J=25C, V_{DD}=-15V, V_G=-10V, R_G=25ohm, L=0.5mH, I_{AS}=-24.08A, V_{DD}=0V during time in avalanche.
3. $R_{\theta JA}$ is measured with the device mounted on a 1inch² pad of 2oz copper FR4 PCB.
4. Pulse Test: Pulse Width≤300μs, Duty Cycle≤0.5%.

Typical Performance Characteristics

Figure 1: Power De-rating

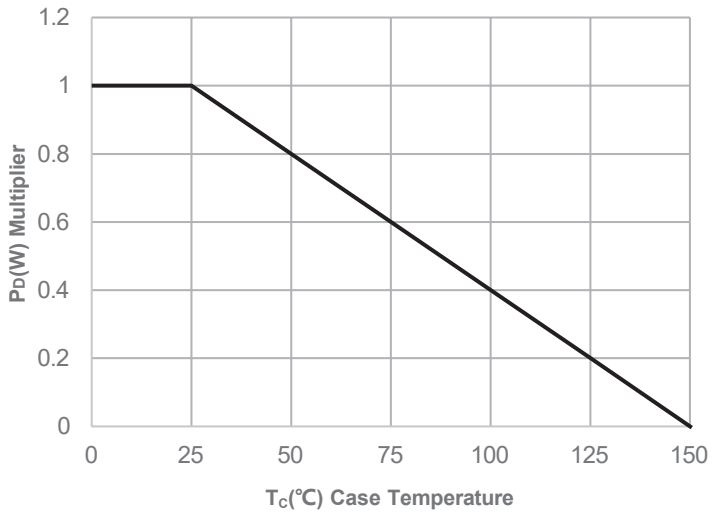


Figure 2: Current De-rating

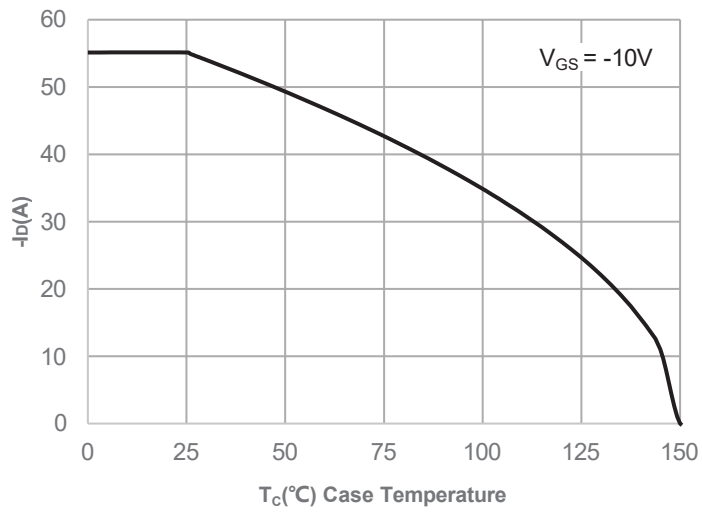


Figure 3: Normalized Maximum Transient Thermal Impedance

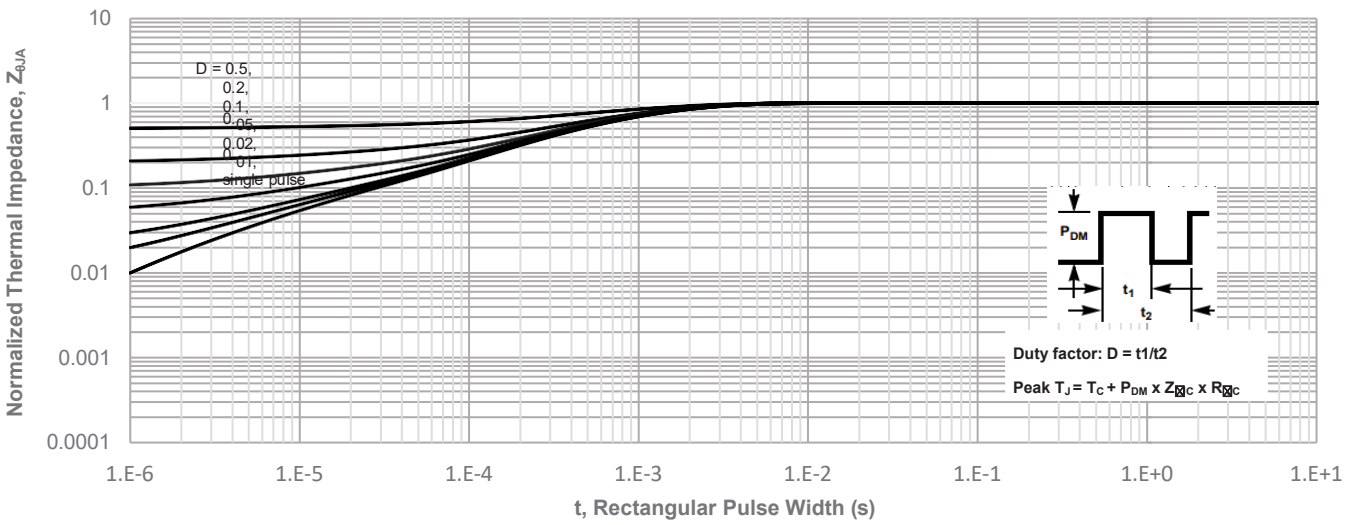
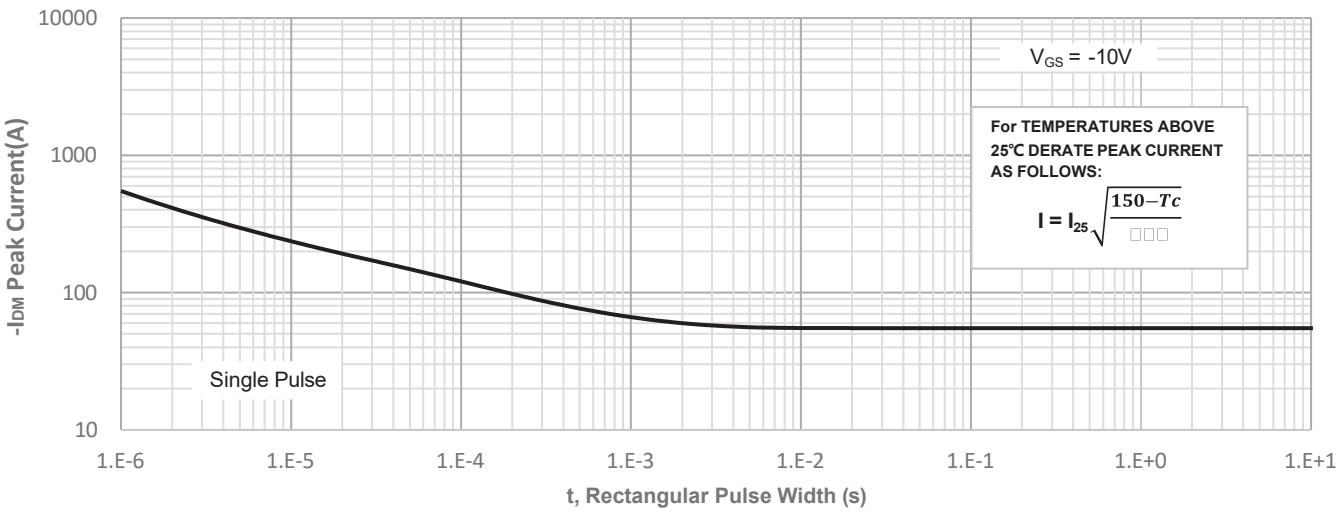


Figure 4: Peak Current Capacity



Typical Performance Characteristics

Figure 5: Output Characteristics

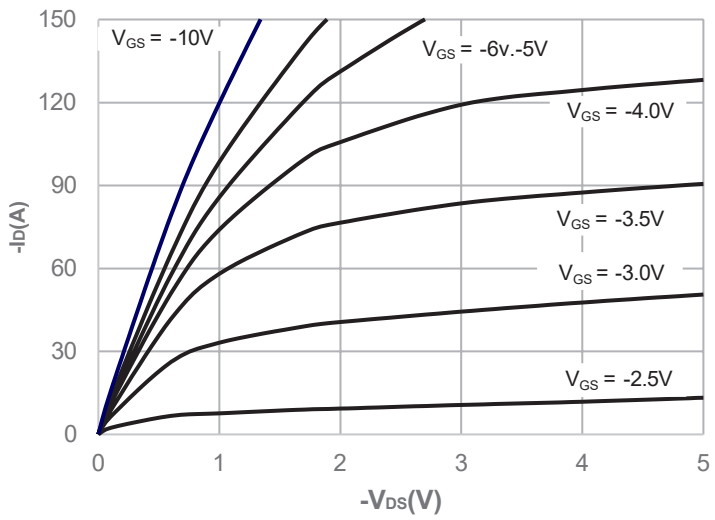


Figure 6: Typical Transfer Characteristics

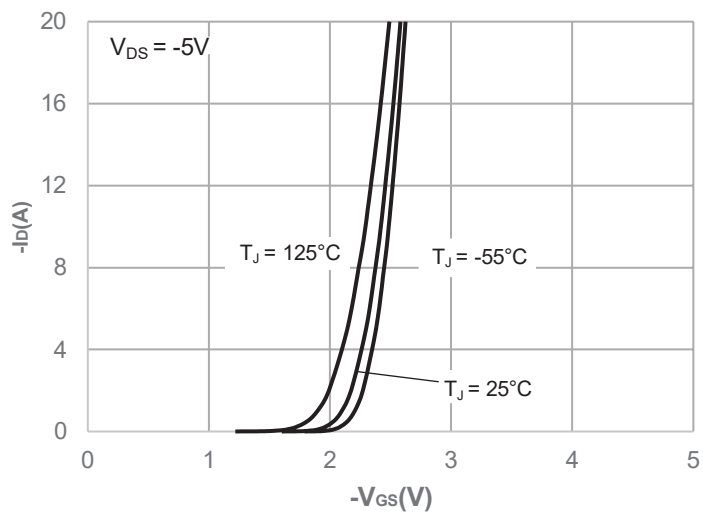


Figure 7: On-resistance vs. Drain Current

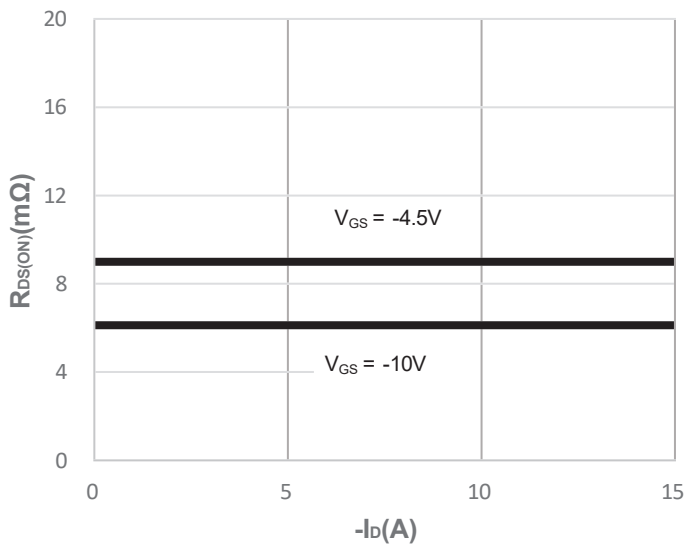


Figure 8: Body Diode Characteristics

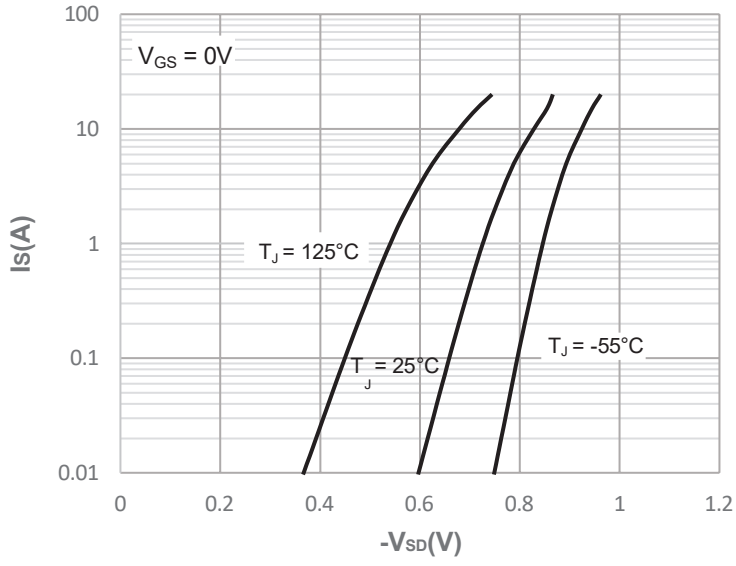


Figure 9: Gate Charge Characteristics

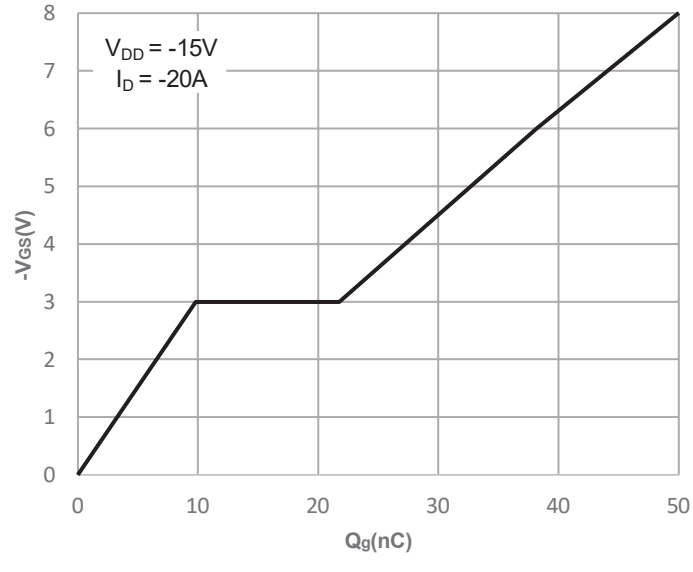
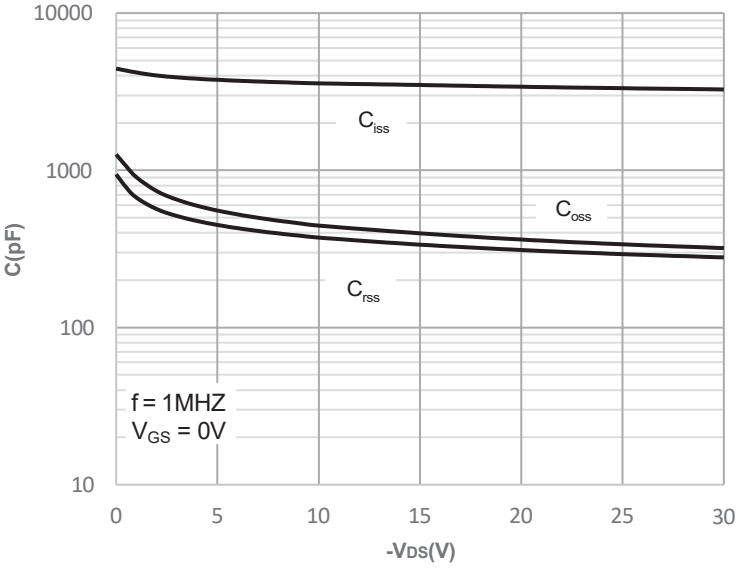


Figure 10: Capacitance Characteristics



Typical Performance Characteristics

Figure 11: Normalized Breakdown voltage vs. Junction Temperature

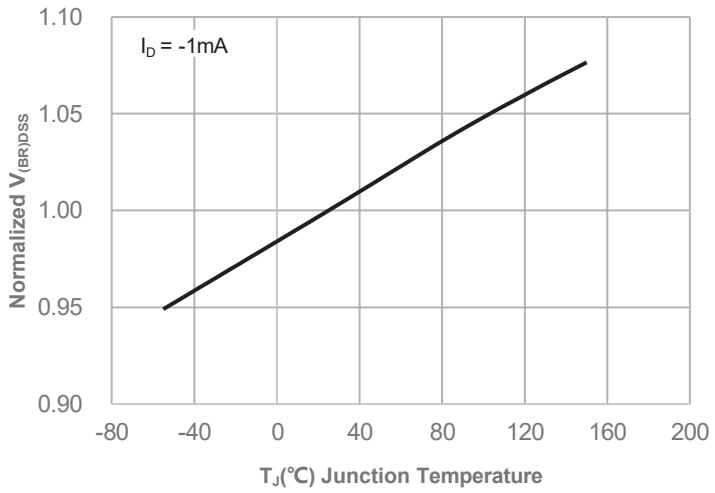


Figure 12: Normalized on Resistance vs. Junction Temperature

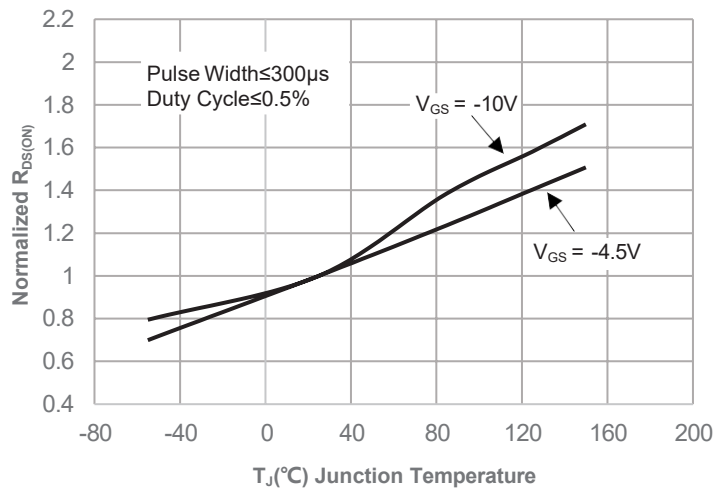
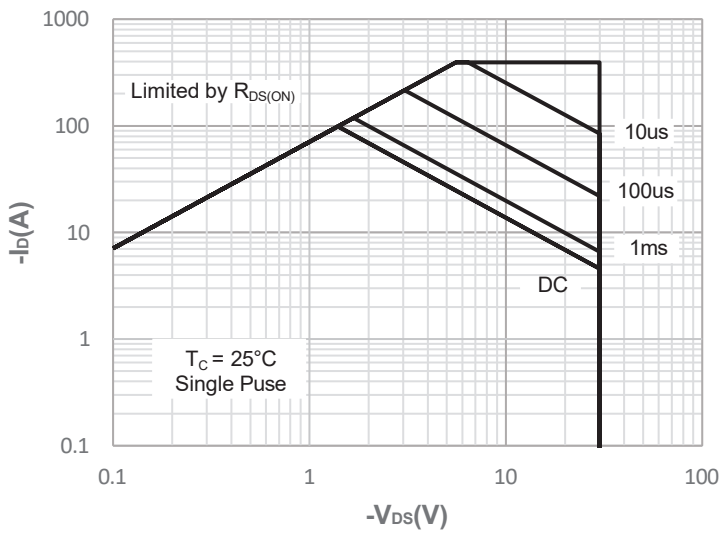


Figure 13: Normalized Threshold Voltage vs. Junction Temperature

Figure 14: $R_{DS(ON)}$ vs. V_{GS}

Figure 15: Maximum Safe Operating Area



Test Circuit

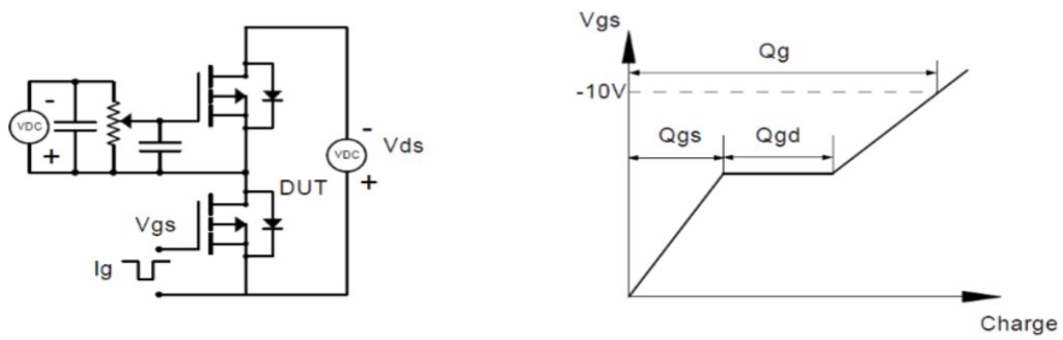


Figure 1: Gate Charge Test Circuit & Waveform

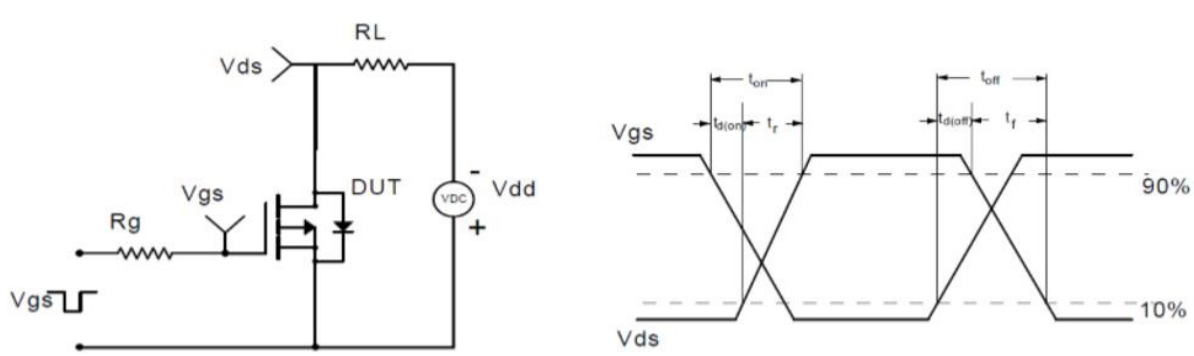


Figure 2: Resistive Switching Test Circuit & Waveform

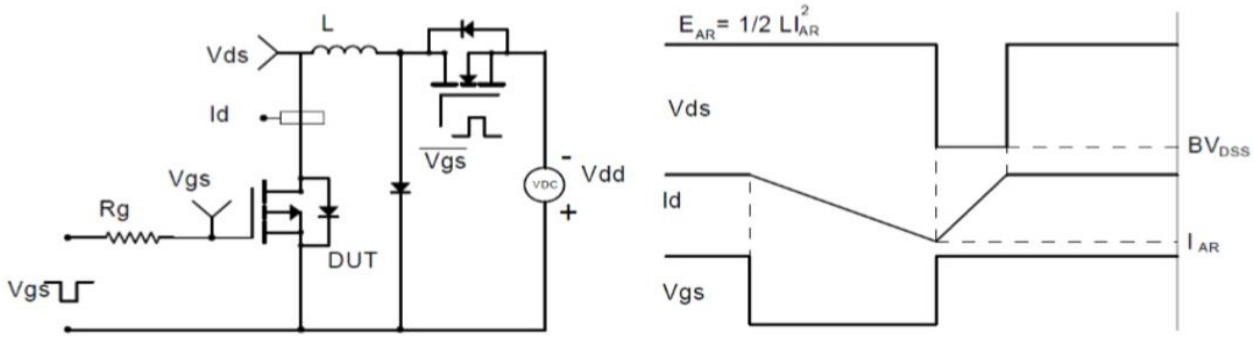


Figure 3: Unclamped Inductive Switching Test Circuit& Waveform

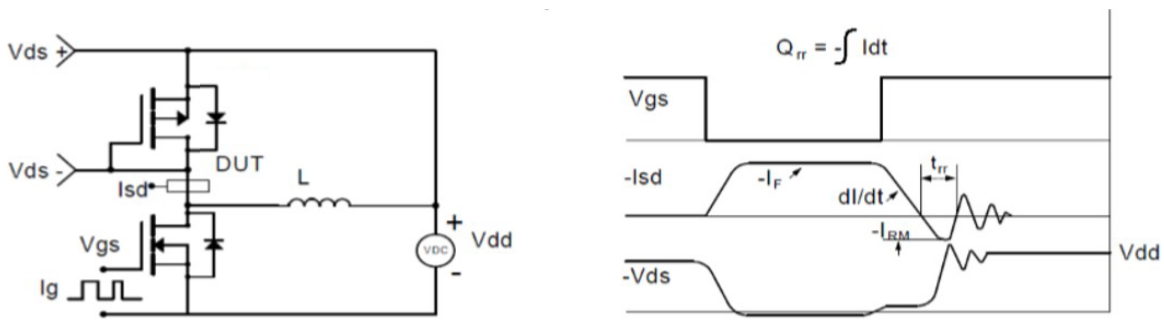


Figure 4: Diode Recovery Test Circuit & Waveform