VS6376, VS7500S, VS75L00S Family

Low-dropout voltage regulators

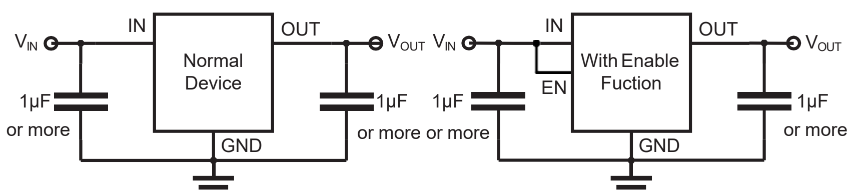
1 Introduction

The VS6376, VS7500S and VS75L00S family are a group of positive voltage regulators manufactured in CMOS technology with ultra low power consumption current. Their input voltage can reach 36V and can provide an output current of up to 300mA, even if the voltage difference between the input and output is small, they can still provide a large output current. They also incorporate a fold-back current limit, short circuit protection and thermal shutdown protection inside the device. Therefore, they are ideal for applications that require quiet power, such as radio frequency (RF) applications, battery-powered devices and so on.

2 Available Packages

PART NUMBER	PACKAGE
VS6376 Series	SOT-23
	SOT-223
	SOT-23-3L/5L
VS7500S Series	SOT-89-3L
VS75L00S Series	SOT-23
	SOT-89-3L

Note: For all available packages, please refer to the part *Orderable Information*.



Typical Application Circuits

3 Features

- Input Voltage Range: 2.5V ~ 36V
- Fixed Output Voltage Available from 1.2V to 12V
- Output Voltage Tolerance:
  - VS6376 Series:
    ±2.5% for Conventional Device
    ±1.0% can be Customized
  - VS7500S Series:
    Available in ±2.5% and ±1% Grade
  - VS75L00S Series:
    Available in ±2.5% and ±1% Grade
- Output Current: up to 300mA
- Low Quiescent Current: 2.5μA (Typ.)
- Dropout Voltage:
  300mV@100mA (V_{OUT} = 3.3V)
- Low Output Noise:
  27×V_{OUT} μV_{RMS} (10Hz ~ 100kHz)
- Power Supply Rejection Ratio:
  70dB@1kHz
- Excellent Transient Response
- Integrated Fault Protection:
  - Fold-back Current Limit
  - Thermal Shutdown
  - Short-circuit Protection

4 Applications

- Car Navigation Systems
- Cordless Phones
- LAN Cards
- Laptop, Palmtops and PDAs
- PC Peripherals with Memory
- Portable Audio Video Equipments
- Radio Control Systems
- Single-lens Reflex DSC
- Ultra Low Power Microcontrollers
- Wireless Communication Equipments

7 Specifications

7.1 Absolute Maximum Ratings

(T_A = 25°C, unless otherwise specified)

CHARACTERISTIC		SYMBOL	VALUE	UNIT
Input voltage range(2)		V_{IN}	-0.3 ~ 40	V
Enable input voltage range(2)		V_{EN}	-0.3 ~ 40	
Output voltage range(2)		V_{OUT}	-0.3 ~ 13	
Maximum power dissipation	VS6376 Series	$P_{D\ Max}$	Internally Limited(3)	W
	VS7500S Series			
	VS75L00S Series			
Maximum junction temperature		$T_{J\ Max}$	150	°C
Storage temperature		T_{stg}	-60 ~ 150	°C
Soldering temperature & time		T_{solder}	260°C, 10s	-

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to network ground terminal.
(3) Refer to *Thermal Information* for details.

7.2 Recommended Operating Conditions

PARAMETER	SYMBOL	MIN.	NOM.	MAX.	UNIT
Input voltage	V_{IN}	2.5	-	36	V
Operating junction temperature	T_J	-40	-	125	°C
Operating ambient temperature	T_A	-40	-	85	°C

7.3 ESD Ratings

ESD RATINGS		SYMBOL	VALUE	UNIT
Electrostatic discharge(4)	Human body model	$V_{ESD\text{-}HBM}$	4000	V
	Machine model	$V_{ESD\text{-}MM}$	200	

(4) ESD testing is conducted in accordance with the relevant specifications formulated by the Joint Electronic Equipment Engineering Commission (JEDEC). The human body model (HBM) electrostatic discharge test is based on the JESD22-114D test standard, using a 100pF capacitor and discharging to each pin of the device through a resistance of 1.5kΩ. The electrostatic discharge test in mechanical model (MM) is based on the JESD22-115-A test standard and uses a 200pF capacitor to discharge directly to each pin of the device.

7 Specifications

7.4 Thermal Information

THERMAL METRIC(5)	SYMBOL	VS6376, VS7500S, VS75L00S Family				UNIT
Junction-to-ambient thermal resistance	$R_{\Theta JA}$	**SOT-23**	**SOT-23-3L**	**SOT-89-3L**	**SOT-223**	°C/W
		357.2	261.1	160.6	99.5	
		SOT-23-5L	-			
		250.3				
Junction-to-case thermal resistance	$R_{\Theta JC}$	**SOT-23**	**SOT-23-3L**	**SOT-89-3L**	**SOT-223**	°C/W
		136.4	67.0	52.9	19.6	
		SOT-23-5L	-			
		65.4				
Reference maximum power dissipation for continuous operation	$P_{D\ Ref}$	**SOT-23**	**SOT-23-3L**	**SOT-89-3L**	**SOT-223**	W
		0.28	0.38	0.63	1.00	
		SOT-23-5L	-			
		0.40				

(5) Thermal metric is measured in still air with T_A = 25°C and mounted on a 1 in^2 FR-4 substrate PCB covered with 2 ounces of copper.

7 Specifications

7.5 Electrical Characteristics

VS6376, VS7500S and VS75L00S Family (V_{IN} = V_{OUT} +1V, C_{IN} = 1.0μF, C_{OUT} = 1.0μF, T_A = 25°C, unless otherwise specified)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		MIN.	TYP.[6]	MAX.	UNIT
Input voltage	V_{IN}	-		2.5	-	36	V
DC output tolerance	-	T_J = 25°C, I_{OUT} = 1mA		-2.5[7]	-	2.5[7]	%
				-1[7]	-	1[7]	
Available output voltage	-	-		2.1	-	12	V
Output current	I_{OUT}	T_J = 25°C		300	-	-	mA
Quiescent current	I_Q	I_{OUT} = 0mA	V_{OUT} < 7.0V	-	2.5	6.0	μA
			V_{OUT} > 7.0V	-	3.5	7.0	
Dropout voltage	V_{DO}[8]	V_{OUT} = 3.0 to 3.6V	I_{OUT} = 100mA	-	300	-	mV
		V_{OUT} = 5.0V		-	250	-	
		V_{OUT} = 12V		-	200	-	
Line regulation	LNR[9]	V_{IN} = V_{OUT} +1V to 36V, I_{OUT} = 10mA		-	0.01	0.3	%/V
Load regulation	ΔV_{LOAD}	V_{IN} = V_{OUT} +1V, I_{OUT} = 1 to 100mA		-	10	-	mV
Temperature characteristics	TR[10]	I_{OUT} = 10mA, T_A = -40 to 85°C		-	50	-	ppm/°C
Output current limit	I_{Limit}	V_{OUT} = 0.5 × $V_{OUT\ Normal}$, V_{IN} = 5.0V		350	600	-	mA
Short current	I_{Short}	OUT short to GND		-	100	-	mA
Standby current	I_{STBY}	EN = GND		-	-	0.5	μA
Power supply rejection ratio	PSRR	I_{OUT} = 50mA, V_{IN} = (V_{OUT} +1.5V) DC + $1V_{PP\ AC}$	f = 100Hz	-	75	-	dB
			f = 1kHz	-	70	-	
			f = 10kHz	-	55	-	
			f = 100kHz	-	40	-	
Output noise voltage	V_N	BW = 10 to 100kHz		-	27 × V_{OUT}	-	$μV_{RMS}$
EN high	$V_{EN\ H}$	-		1.5	-	V_{IN}	V
EN low	$V_{EN\ Low}$	-		-	-	0.3	V
C_{OUT} auto-discharge resistance	$R_{Discharge}$	V_{IN} = 5.0V, V_{OUT} = 3.0V, EN = GND		-	150	-	Ω
Thermal shutdown	T_{SD}	-		-	160	-	°C
Thermal shutdown hysteresis	ΔT_{SD}	-		-	20	-	°C

7 Specifications

7.5 Electrical Characteristics (continued)

Note:

(6) Typical numbers are at 25°C and represent the most likely norm.

(7) ±1% grade products are available for VS7500S and VS75L00S series, they can also be customized for VS6376 series.

(8) Test the difference of output voltage and input voltage when input voltage is decreased gradually till output voltage equals to 98% of $V_{OUT\ Normal}$.

(9) The line regulation is calculated by the following formula:

$$\square\square\square = \frac{\Delta V_{OOUT}}{\square_{\square\square\square\square} \times \Delta V_{\square\square}}$$

where, ΔV_{OUT} is the variation of the output voltage, ΔV_{IN} is the variation of the input voltage.

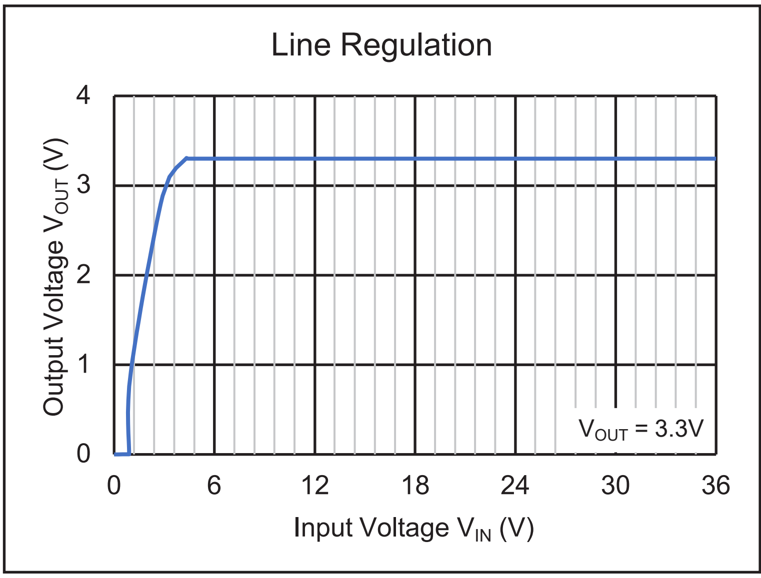
(10) The output voltage temperature characteristics (TR) is calculated by the following formula:

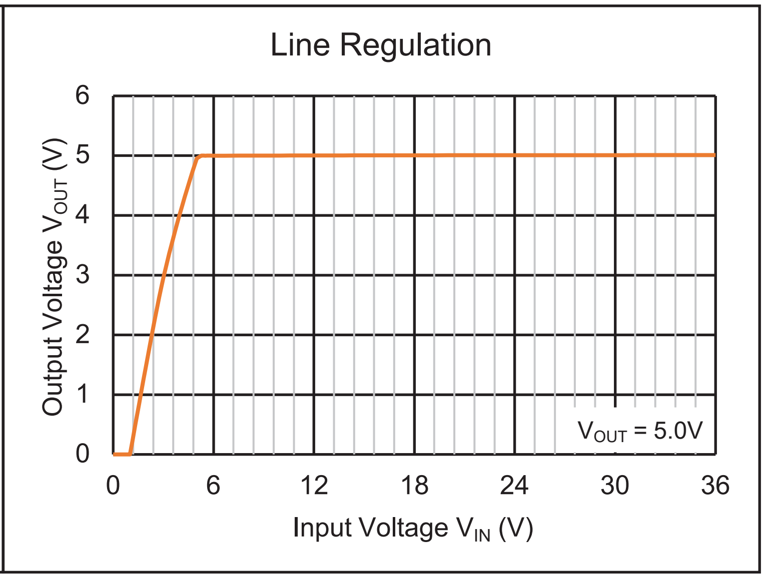
$$\square\square = \frac{\Delta V_{OOUT}}{\square_{\square\square\square\square} \times \Delta T}$$

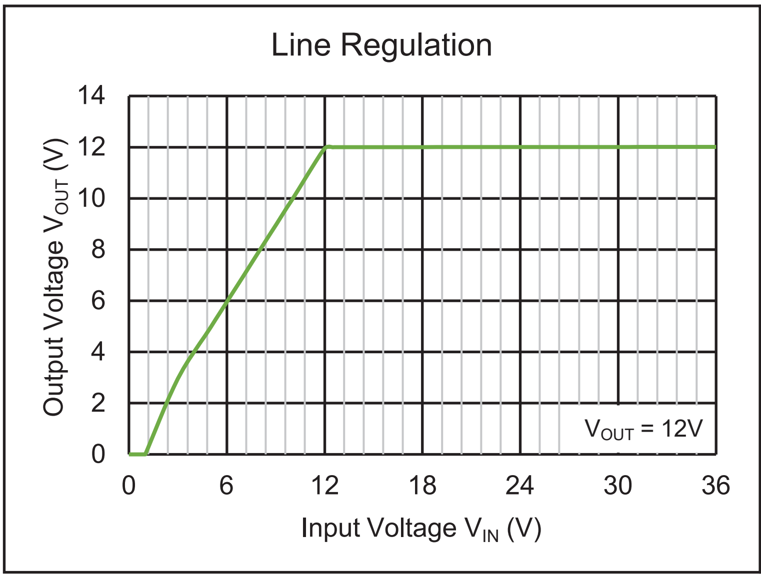
where, ΔV_{OUT} is the variation of the output voltage, ΔT is the variation of the ambient temperature.

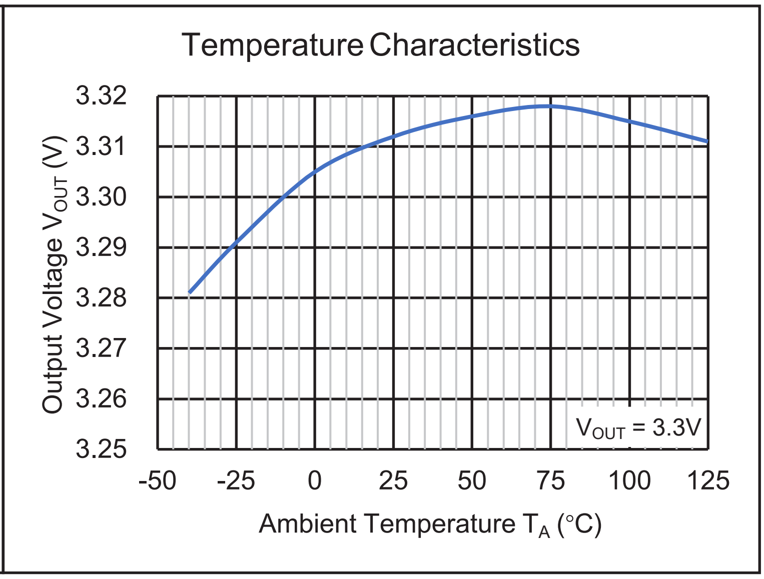
7.6 Typical Characteristics

VS6376, VS7500S and VS75L00S Family (V_{IN} = V_{OUT} +1V, I_{OUT} = 10mA, C_{IN} = 1.0µF, C_{OUT} = 1.0µF, T_A = 25°C, unless otherwise specified)





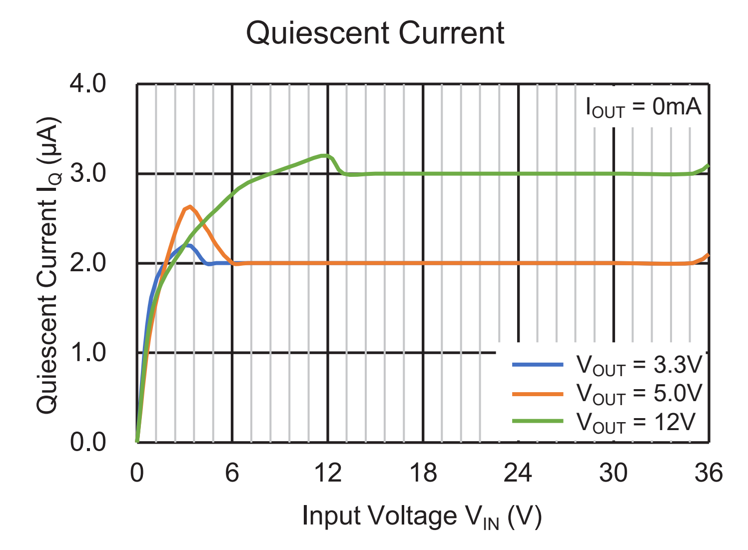


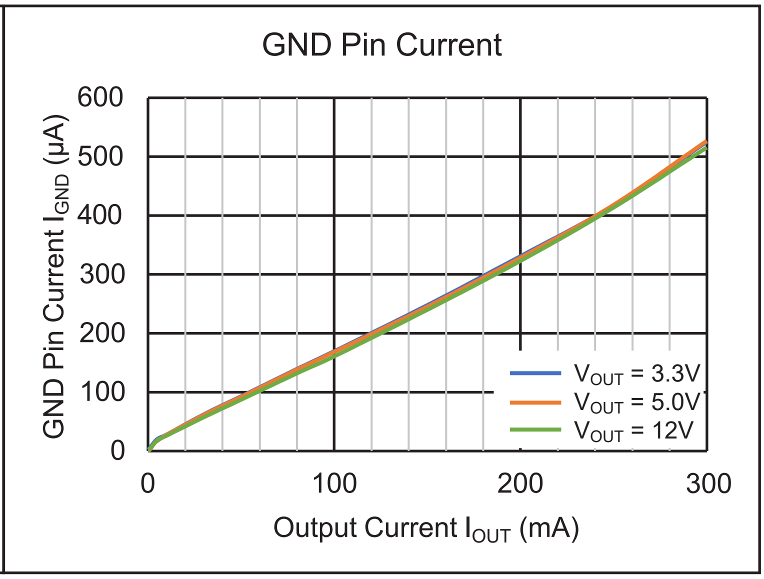


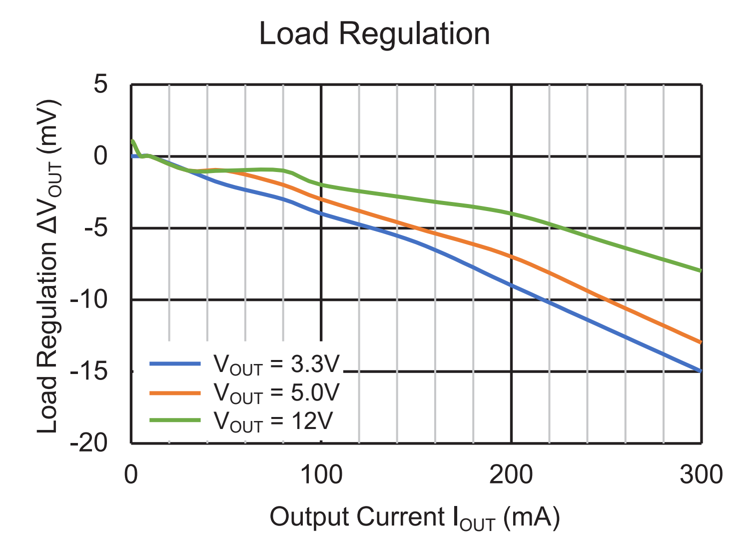
7 Specifications

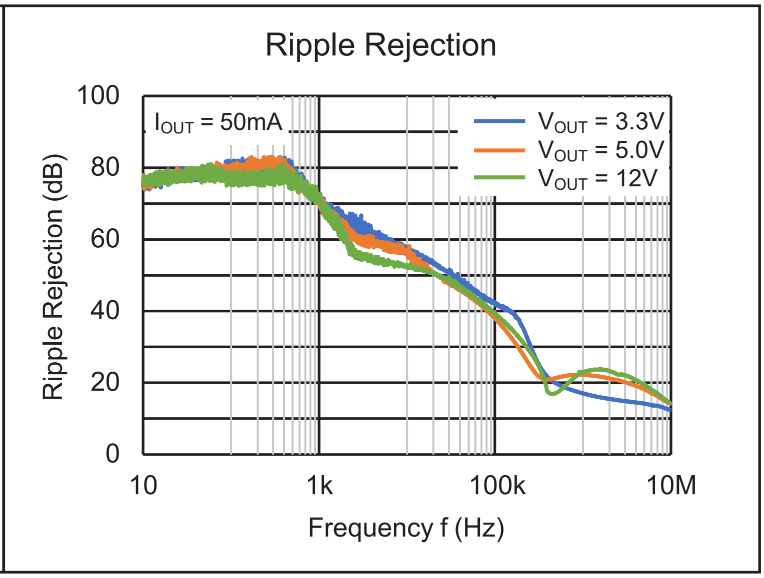
7.6 Typical Characteristics (continued)

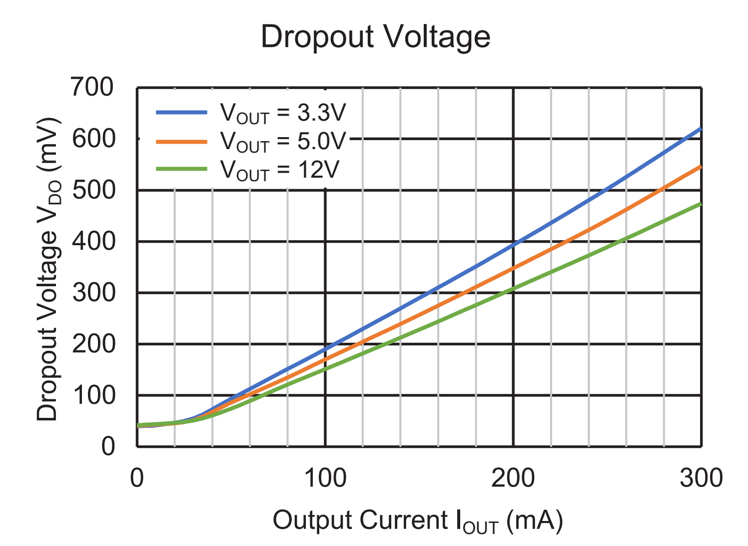
VS6376, VS7500S and VS75L00S Family (V_{IN} = V_{OUT} +1V, I_{OUT} = 10mA, C_{IN} = 1.0µF, C_{OUT} = 1.0µF, T_A = 25°C, unless otherwise specified)

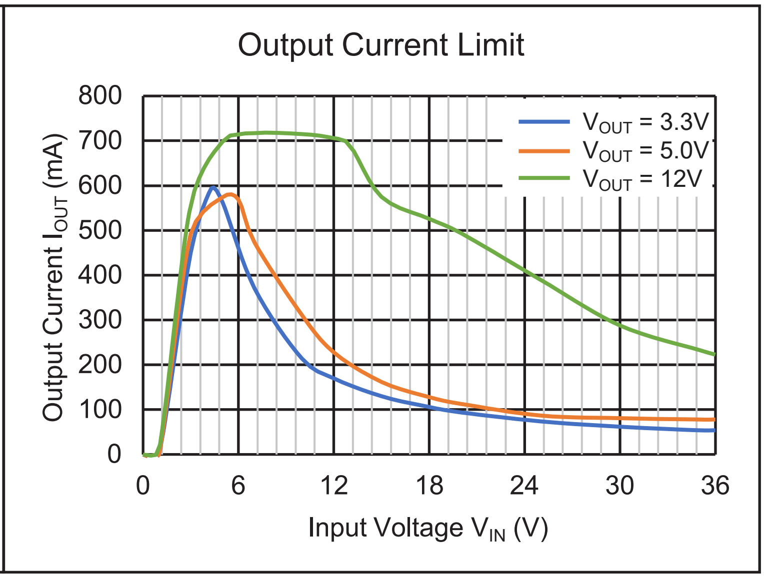












7 Specifications

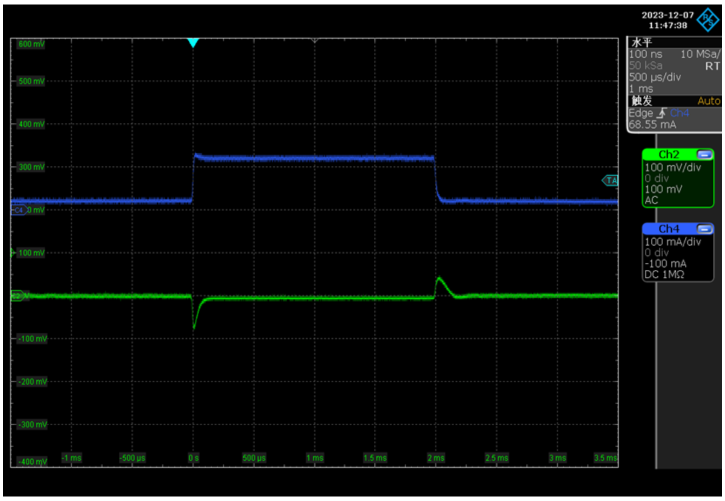
7.6 Typical Characteristics (continued)

VS6376, VS7500S and VS75L00S Family (V_{IN} = V_{OUT} +1V, I_{OUT} = 10mA, C_{IN} = 1.0μF, C_{OUT} = 1.0μF, T_A = 25° C, unless otherwise specified)

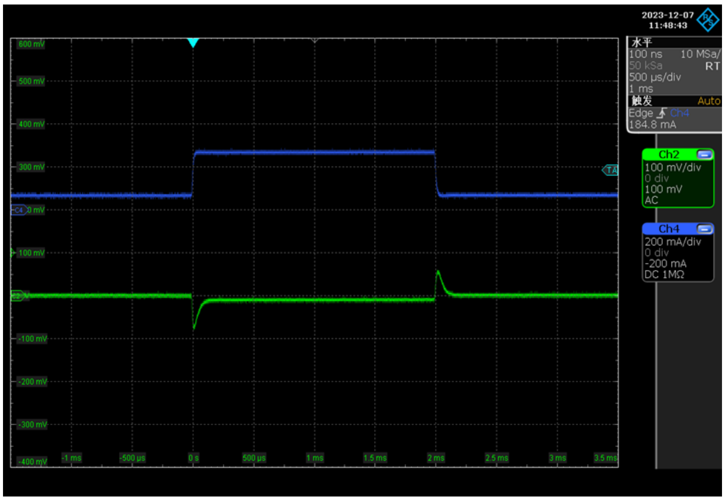
Load Transient

V_{EN} = V_{IN}, V_{IN} = V_{OUT} +1V, CH_2: V_{OUT}, CH_4: I_{OUT}

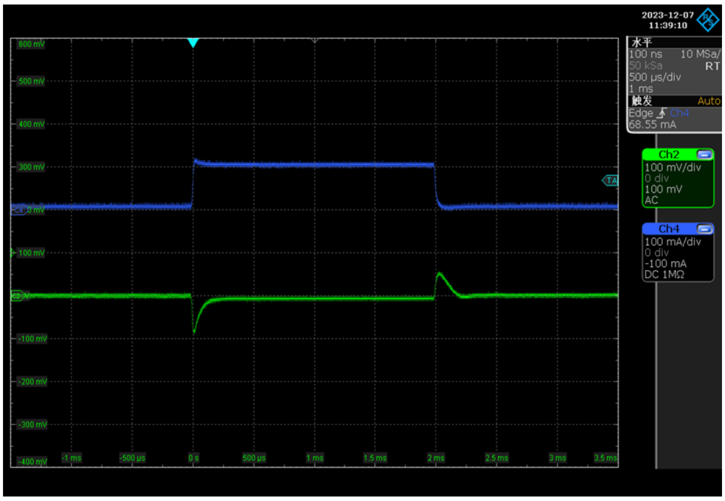
V_{OUT} = 3.3V, I_{OUT} = 1 ~ 100mA



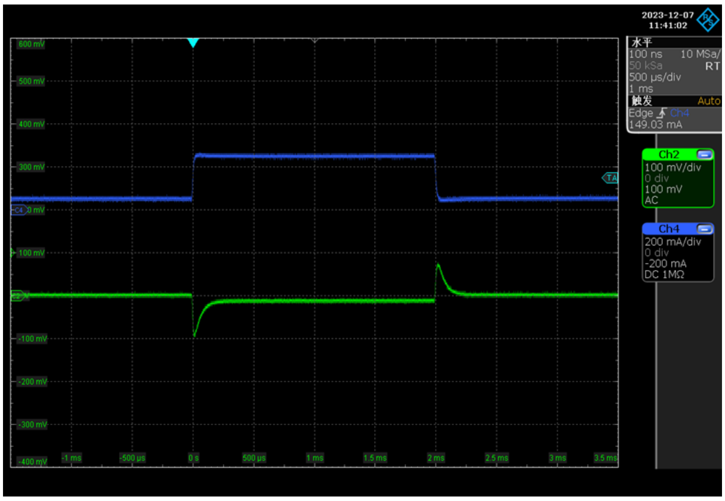
V_{OUT} = 3.3V, I_{OUT} = 50 ~ 250mA



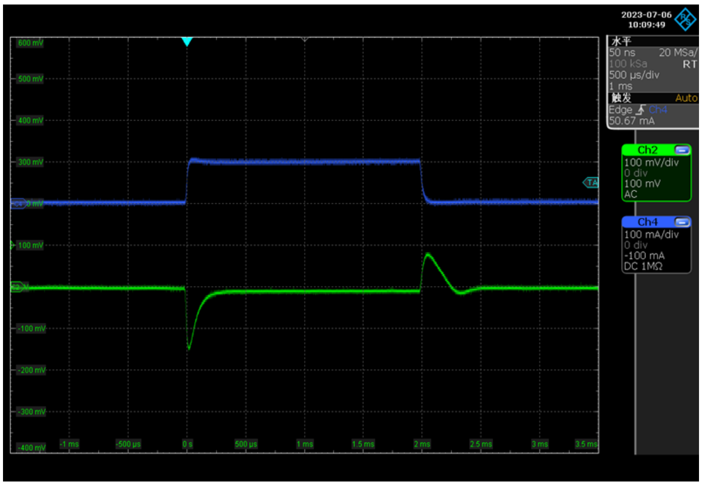
V_{OUT} = 5.0V, I_{OUT} = 1 ~ 100mA



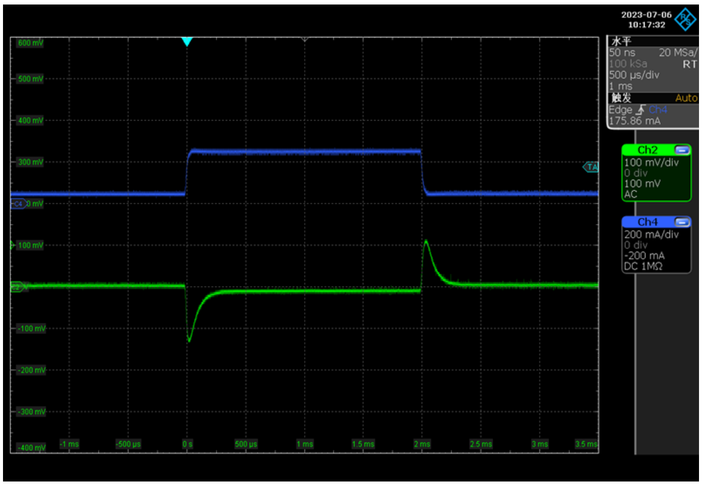
V_{OUT} = 5.0V, I_{OUT} = 50 ~ 250mA



V_{OUT} = 12V, I_{OUT} = 1 ~ 100mA



V_{OUT} = 12V, I_{OUT} = 50 ~ 250mA



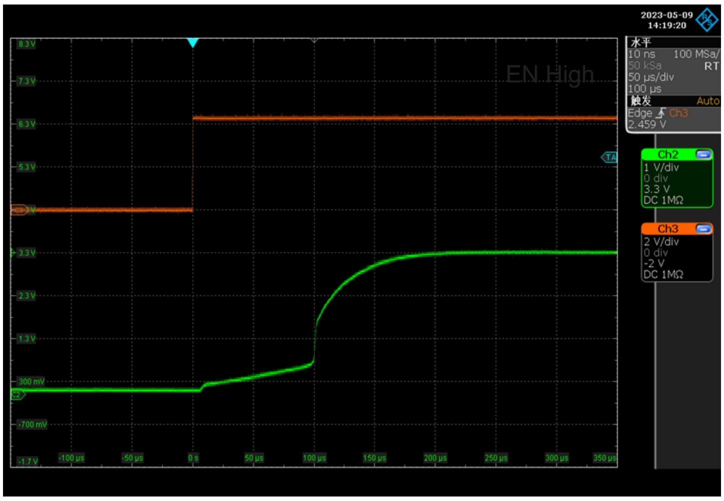
7 Specifications

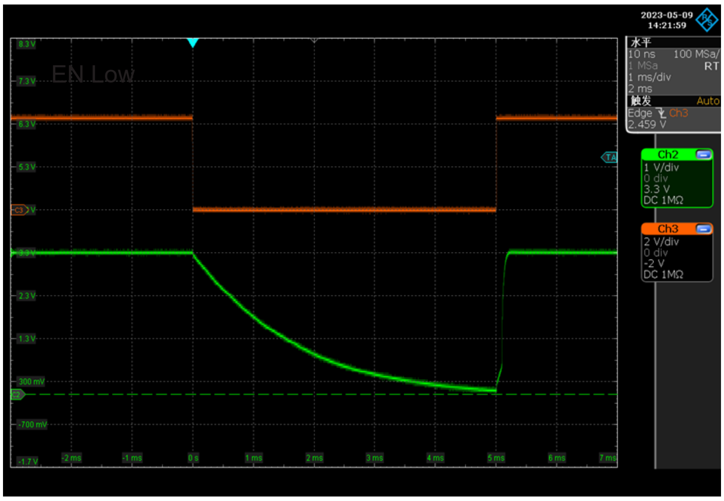
7.6 Typical Characteristics (continued)

VS6376, VS7500S and VS75L00S Family (V_{IN} = V_{OUT} +1V, I_{OUT} = 10mA, C_{IN} = 1.0μF, C_{OUT} = 1.0μF, T_A = 25°C, unless otherwise specified)

EN High & Low

V_{OUT} = 3.3V, V_{IN} = 4.3V, V_{EN} = 0 ~ 4.3V, I_{OUT} = 0mA, CH_2: V_{OUT}, CH_3: V_{EN}

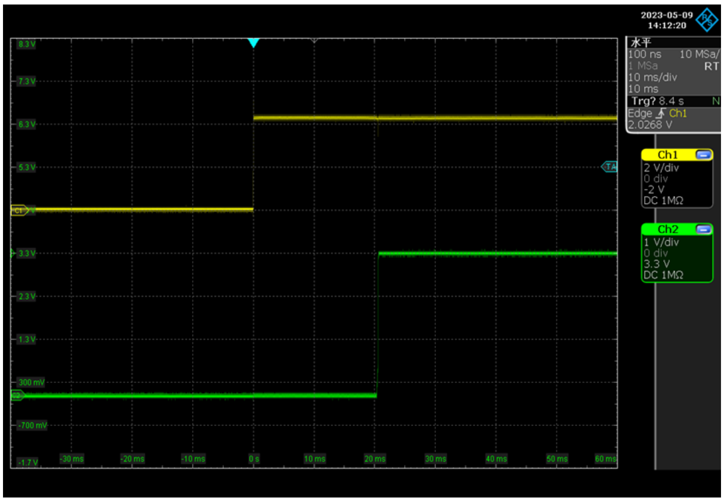




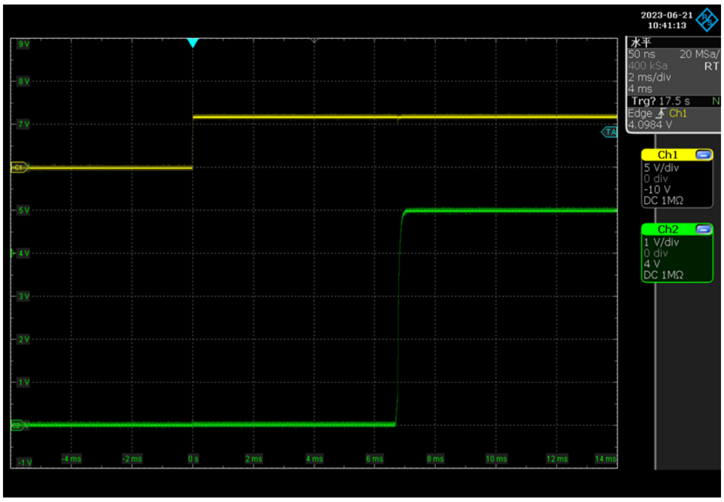
Power on Response

V_{EN} = V_{IN}, I_{OUT} = 10mA, V_{IN} = 0 ~ V_{OUT} +1V, CH_1: V_{IN}, CH_2: V_{OUT}

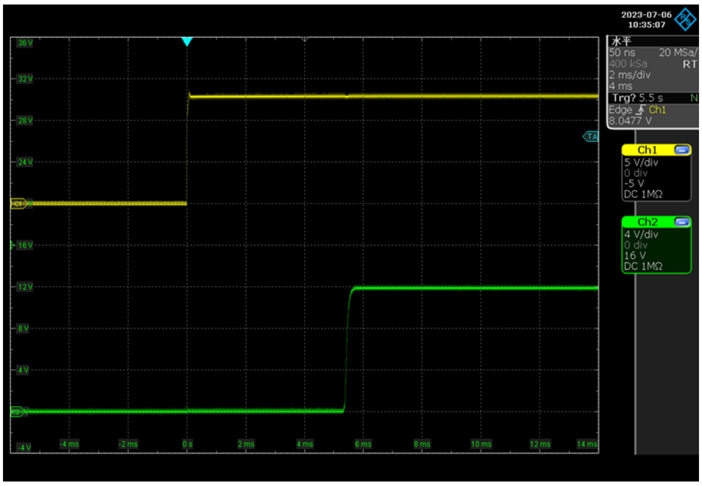
V_{OUT} = 3.3V, V_{IN} = 0 ~ 4.3V



V_{OUT} = 5.0V, V_{IN} = 0 ~ 6.0V



V_{OUT} = 12V, V_{IN} = 0 ~ 13V

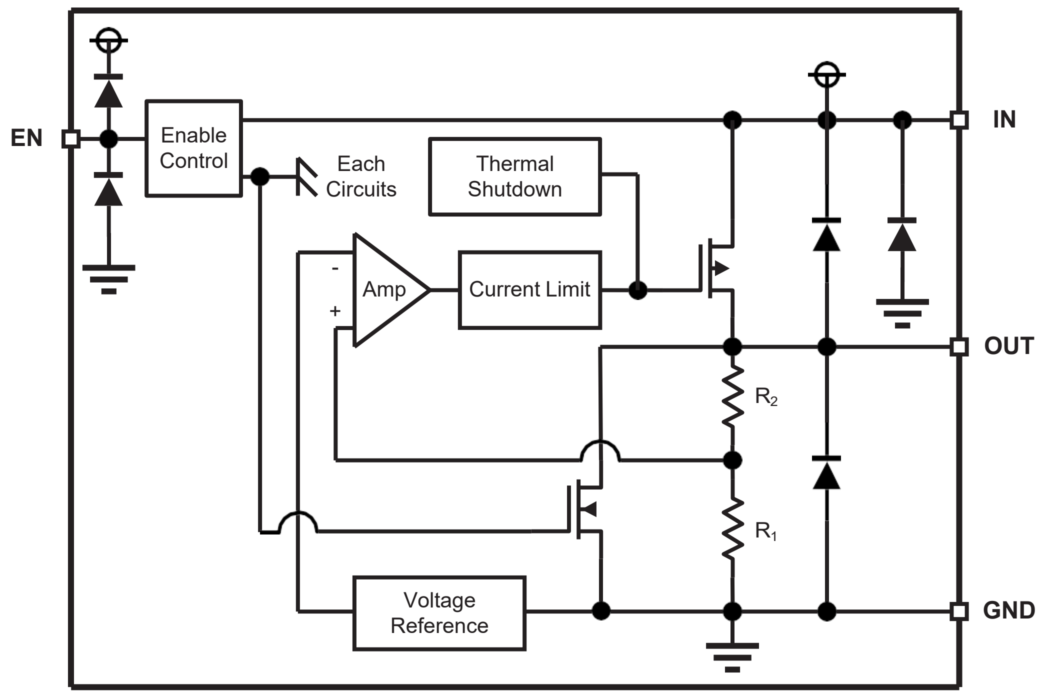


8 Detailed Description

8.1 Description

The VS6376 series, VS7500S series and VS75L00S series are a group of low voltage differential linear regulators with a maximum input voltage of 36V and an output current of 300mA. Their quiescent current is as low as 2.5μA, and internally integrated with fold-back current limit, output short circuit protection, and thermal shutdown protection. Therefore, they are very suitable for uninterrupted power supply system and battery powered devices.

8.2 Functional Block Diagram



The internal feedback resistors R_1 and R_2 form a voltage divider circuit to compare the V_{FB} input error amplifier with the reference voltage. The internal regulator tube (PMOS) will control its conduction degree through the grid voltage provided by the error amplifier output, which will make the output voltage V_{OUT} not affected by temperature changes or input voltage changes to a certain extent, thus maintaining the stability of the device output voltage.

8 Detailed Description

8.3 Feature Description

Power Supply Input

When the input voltage is lower than the rated range of the data sheet, the device will lose the regulation function of stabilizing the output voltage, that is, it is unable to maintain the output voltage within the rated range. At this time, compared with normal operation, the quiescent current of the device may exceed the rated range, and the transient response performance may be seriously degraded.
When the input voltage is higher than the rated range of the data sheet, the device may cause irreversible damage or failure due to exceeding the maximum rated range of electrical stress.
For the rated input voltage of the device, see *Recommended Operating Conditions* and *Dropout Voltage*.

Output Current

When the circuit design is appropriate, the device can reach the maximum load capacity of at least 300mA. According to the power dissipation of the package and the effective connection thermal resistance with the environment, selecting the appropriate package for the circuit design can make the device emit more heat energy.

Built-in Current Limit & Short Circuit Protection

The VS6376 series, VS7500S series and VS75L00S series are designed with internal current limiting circuit, which can protect the device by limiting the load current value in case of instantaneous high load current. When the current limiting is triggered, the output voltage is not regulated. If the out pin of the regulator is short circuited, the internal current limiting circuit will be triggered, the output current of the device will maintain at a relatively small value to protect the device. The typical value of short current I_{Short} can be found in *Electrical Characteristics*. The current limiting state will continue until the load current drops to the normal range.
When the load current of the device is large, the device will generate more heat due to the increase of power consumption, which may cause the device to turn off its output due to the internal thermal shutdown protection before the current limit is triggered.
In order to ensure the normal operation of current limit, the inductance of input and load shall be minimized. Continuous operation under current limit is not recommended.
The current limit mode of these device is fold-back current limit. Please refer to the *Fold-back Current Limit* for more details.

Thermal Shutdown

The VS6376 series, VS7500S series and VS75L00S series are designed with thermal shutdown protection. When the junction temperature (T_J) of the internal main channel MOSFET exceeds the thermal shutdown threshold temperature (T_{SD}), thermal shutdown will be triggered. At this time, the output will be turned off to prevent catastrophic damage to the chip due to accidental heating. When the T_J drops to a certain range of thermal shutdown threshold temperature (ΔT_{SD}), the thermal shutdown will be released and the device will return to the normal output. The temperature threshold of device triggering thermal shutdown (T_{SD}) and temperature range to be lowered to released from thermal shutdown (ΔT_{SD}) can be found in the *Electrical Characteristics*.
To ensure reliable operation, please limit the junction temperature to the specified range of *Recommended Operating Conditions* in the data sheet. Applications that exceed the recommended temperature range may cause the device to exceed its operating specifications.
Although the internal protection circuit of the device is designed to prevent overall thermal conditions, it is not intended to replace proper power dissipation. Running the device continuously until thermal shutdown or higher than the recommended operating T_J will reduce long-term reliability.

8 Detailed Description

8.3 Feature Description (continued)

Dropout Voltage

Dropout voltage (V_{DO}) refers to the minimum voltage difference between input and output (V_{IN} - V_{OUT}) to make the device output voltage reach the rated range at rated current. When the dropout voltage condition required by the device is reached, the internal MOSFET will be fully turned on, at this time, the MOSFET is equivalent to a switch for regulation.
The V_{DO} increases with the increase of load current. Since V_{IN} - V_{OUT} must be no less than the V_{DO}, the V_{DO} indirectly specifies the minimum input voltage of devices under different load current conditions. If the V_{IN} - V_{OUT} is less than the V_{DO}, the performance of the device may deteriorate (see *Operation in Dropout Mode* for details).

Enable Control

The enable pin of the device (EN) is active at high level. When the voltage of the EN is greater than the EN logic high voltage ($V_{EN\ H}$), the device will be enabled and maintain the normal output. When the voltage of the EN is lower than the EN logic low voltage ($V_{EN\ L}$), the internal circuit of the device will be disabled and the output will be turned off the device, the device will be in the standby mode until EN is turned to high level again. The $V_{EN\ H}$ and $V_{EN\ L}$ can be found in the *Electrical Characteristics*.
Normal startup waveform and startup slope rate control can be ensured when the device starts from any low voltage lower than $V_{EN\ L}$, but the discharge time of output capacitor must be taken into account. EN can not be float, if EN is not required to control the output voltage independently, connect EN to IN.

Auto-discharge Function

The device with enable control has an auto-discharge circuit. When the enable control is turned off, the device will be disabled. An internally integrated pull-down MOSFET (see *Functional Block Diagram*) will connect a resistor ($R_{Discharge}$) to the ground to release the charge in the output capacitor, thus closing the entire device circuit. The value of $R_{Discharge}$ can be found in the *Electrical Characteristics*. The discharge time of the output capacitor after the device is disabled is determined by the output capacitance (C_{OUT}) and load resistance (R_L) in parallel with the $R_{Discharge}$. The time constant τ can be calculated by the following formula:

$$\tau = C \times R_{Discharaae} \ (R_L = 0)$$

$$\tau = C \times \left(\frac{R_L \times R_{Discharaae}}{\square_{\square} + R_{Discharaae}}\right) \ (R_L \neq 0)$$

The output voltage after discharging through pull-down MOSFET can be calculated by the following formula:

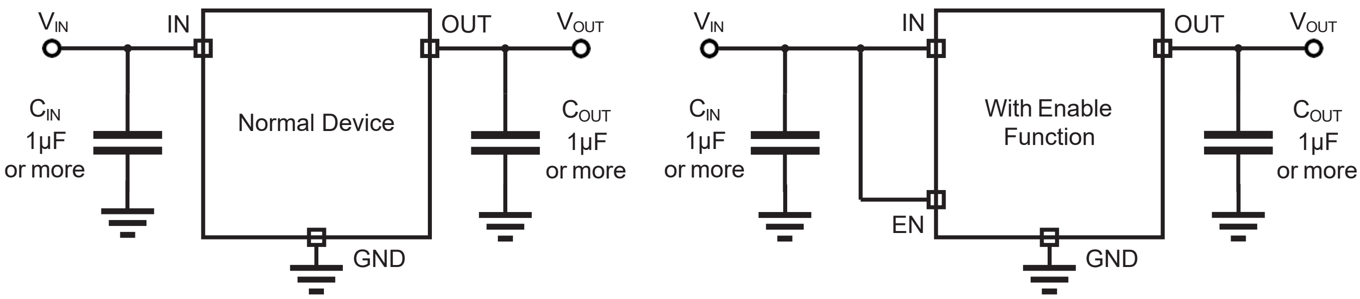
$$V = V_{OOUT} \times ee^{-\frac{\square}{\tau}}$$

$$t = \tau \times \ln\left(\frac{\square}{\square_{\square\square\square\square}}\right)$$

Where, V is the output voltage after discharge, V_{OUT} is the output voltage, t is the discharge time, τ is the discharge time constant.
Do not rely on the active discharge circuit to release a large amount of output capacitance after the input power supply crashes, because the reverse current can flow from the output to the input. This reverse current may damage the device. The limiting reverse current shall not exceed 5% of the rated current of the device.

9 Application and Implementation

9.1 Typical Application Circuits



9.2 Application Information

Selection of Bypass Capacitances

For the VS6376 series, VS7500S series and VS75L00S series, it is recommended to use 1μF or more input (C_{IN}) and output (C_{OUT}) ceramic capacitors.

Type of Capacitors:

Since any leakage of the capacitor will increase the quiescent power consumption of the whole circuit, attention should be paid to selecting capacitors with low leakage. When designing the circuit of portable equipment, due to the shortage of tantalum capacitors, it is a good choice to use small size, low equivalent series resistance (ESR) and high RMS current capacity multilayer ceramic capacitors (MLCC) in the DC to DC voltage conversion. The designer must choose the appropriate capacitor type for circuit design: X7R- ceramic capacitors of X5R- and COG-rated dielectric materials can provide relatively good capacitance stability within the temperature range, Y5V- type capacitors are not recommended because of large changes in capacitance values. However, no matter which type of ceramic capacitor is selected, the effective capacitance may vary with the operating voltage and temperature. The designer must consider the influence of the change of the effective value of capacitance according to the circuit design and application conditions.

Input Capacitors (C_{IN}):

It is recommended to use a 1μF or more capacitor at the input pin of the device, and the position of the input capacitor should be as close to the device input pin as possible.

The input capacitor is not necessary to maintain the output stability, but it can offset the reactive input source and improve the transient response, input ripple and PSRR performance of the device. It should be noted that although many types of capacitors can be used for input bypass, using ceramic capacitors for input filtering may cause problems. Due to the self resonance and high Q characteristics of some types of ceramic capacitors, under certain starting conditions, applying voltage steps to ceramic capacitors may lead to large current surges (such as directly connecting the input pin of LDO to the power supply), which may cause some energy stored in the parasitic inductance of the power lead. When the stored energy is transferred from these inductors to ceramic capacitors, large voltage spikes may occur in the circuit. These voltage spikes are easily twice the step amplitude of the input voltage, and are likely to bring potential risks to the normal operation and reliability of the device. Therefore, the selection of ceramic capacitors as input capacitors must be careful. Adding 3Ω resistors and X5R- type ceramic capacitors will minimize voltage transients during startup. A higher value capacitor may be necessary if large, fast rise-time load or line transients are anticipated or if the device is located several inches from the input power source.

9 Application and Implementation

9.2 Application Information (continued)

Selection of Bypass Capacitances (continued)

Output Capacitors (C_{OUT}):

Recommended 1μF or more output ceramic capacitor to keep the device output stable, and the capacitor position should be as close to the device pin as possible.

The device needs an output capacitor to achieve loop stability. As with any regulator, a larger output capacitance reduces the peaks during a load transient but slows down the response time of the device. The proper capacitor can help to obtain better dynamic performance.

Transient Response

Transient response refers to the change of system output from initial state to stable state under the action of typical signal input. For LDO, the designer should pay attention to the possible impact of linear transient response and load transient response on the system: linear transient response refers to the transient response of output to change when the input voltage changes, while load transient response refers to the transient response of output to change when the output current changes. The specific phenomenon is that the output voltage of the device will have a short spike, especially when the input voltage or output current changes greatly in a short time. This change is not only related to the performance of the chip itself, but also related to the change of output current, change rate and output capacitance:

1. When the output current increases, the output voltage of the device will decrease to a certain extent, and the larger output current will provide a higher current discharge path for the output capacitor, which will affect the peak value generated by the transient spike and reduce the peak value;
2. The output current or input voltage changes relatively slowly, and the output change of the device is relatively small, affecting the spike caused by the change;
3. The use of large input and output capacitors can reduce the spike caused by transient response to a certain extent to improve the transient performance, but large output capacitors can also affect the response time of devices.

For the selection of bypass capacitance value, refer to the *Section of Bypass Capacitances* selection.

Operation in Dropout Mode

These devices are internally integrated with a P-MOSFET to achieve low dropout voltage. The voltage difference between the input and the output (V_{IN} - V_{OUT}) of the device must not be lower than the corresponding dropout voltage (V_{DO}) to ensure that the output voltage tolerance is within the rated range of the data sheet. The dropout voltage will increase with the increase of load current. When the V_{IN} - V_{OUT} is less than the V_{DO}, the P-MOSFET inside the device is in a linear state, the resistance from the input pin to the output pin is equal to the resistance from the drain to the source of the P-MOSFET, and the device functions like a resistor. When operating in this state, the response time of the error amplifier inside the device will be limited, which will seriously degrade the transient performance of the device, when the external circuit has a transient change, the deviation of the output voltage will become larger than the normal operating state. In addition, the PSRR and noise performance of the device will be worse than that under normal operating conditions.

9 Application and Implementation

9.2 Application Information (continued)

Fold-back Current Limit

The VS6376 series, VS7500S series and VS75L00S series adopt the fold-back current limit. The following is some application information of the fold-back current limit.

Current Limit Type:
Current limit can impose certain restrictions on the current value provided by the device. Compared with the so-called "brick-wall" current limiting mode, the significant difference of the fold-back current limit is that overload and short circuit are obviously different. Figure 9-1 and Figure 9-2 show the typical operating characteristics of these two current limiting mechanisms.

1. Operating characteristic curve R1 represents the curve of linear resistance as load under normal working condition;
2. When the linear resistance as the load gradually decreases and causes the device to enter the overload state, the operating characteristic curve is shown in R2;
3. When the linear resistance decreases to 0Ω, the device will enter the short-circuit state, and the operating characteristic curve is shown in R3.

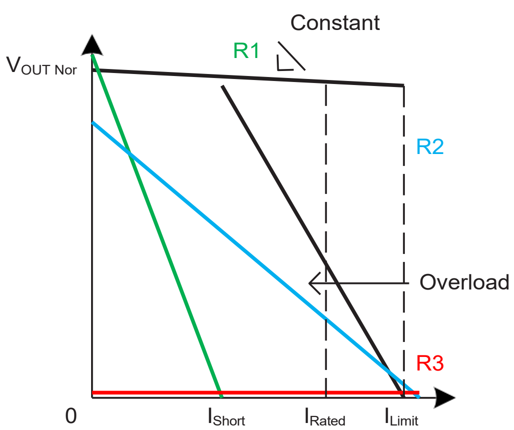


Figure 9-1. Fold-back Current Limit

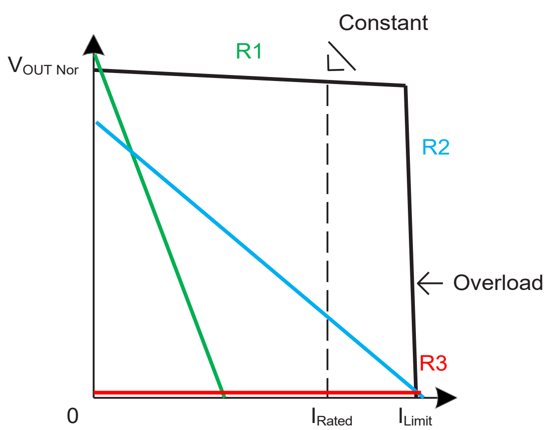


Figure 9-2. Brick-wall Current Limit

After entering the short circuit state, the short-circuit current of the "brick-wall" type current limiting mechanism is limited to I_{Limit}, and the reliability and stability of the voltage regulator may be affected due to the large amount of heat generated during the short circuit, while the I_{Short} of fold-back current limit in the short circuit state is far lower than I_{Limit}, which can reduce the heat energy generated due to power dissipation during the device short circuit. The fold-back current limit allows the device to limit the short circuit current to a small current value without losing the rated range of output current. This is very important if continuous short circuit faults need to be solved.
The current limiting mechanism limits the maximum load current of the device, and the internal transmission transistor of the device will not move outside its safe operation area (SOA) during operation. See *Recommended Continuous Operating Areas* for details.

9 Application and Implementation

9.2 Application Information (continued)

Fold-back Current Limit (continued)

Usage and Precautions:

When using the voltage regulator with the fold-back current limit, it should be noted that the device cannot be started normally under certain loads because the short-circuit current of the fold-back current limit is obviously different from the maximum load current. As shown in the curves S1 and S2 in Figure 9-3, the nonlinear load S1 is distributed in the range of the load curve region where the device can work, because the current provided by the device is always greater than the requirements of the load under all voltage conditions, the device can start normally, and the output will reach the ideal operating point P1; The situation of nonlinear load S2 is different, during actual startup, when the voltage and current are gradually rising, the output of S2 will be limited at P2, because the device cannot provide more current under the voltage at P2, which will make the output stuck at the intersection and maintain at this level, and the device cannot reach the ideal operating point P3 for normal startup.

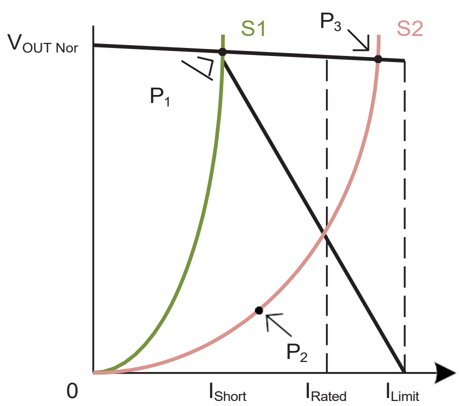


Figure 9-3. Nonlinear Load Example

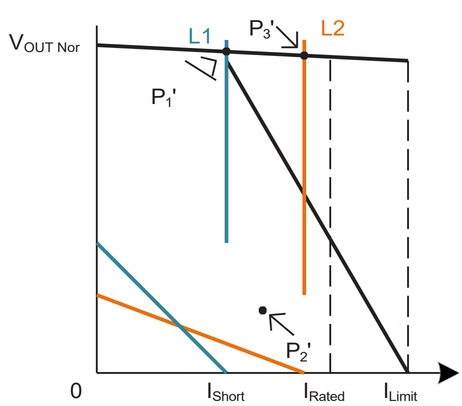


Figure 9-4. Active Load Profile

In addition, many typical cases of actual loads have operating characteristics as shown in L1 and L2 curves in Figure 9-4. When the device starts from zero with L1 and L2 as loads, the load will behave as a linear resistance, and the load current will change to a constant value after reaching the inflection point voltage. Like nonlinear loads S1 and S2, when L1 is used as the load, the device can start normally and reach the ideal working point P1', while when L2 is used as the load, the device cannot start normally, and the output will be stuck at P2' and cannot reach the ideal working point P3'.

As an active load, the electronic load has the same operating characteristics as L1 and L2. Some problems may occur when using the electronic load to test the voltage regulator with a fold-back current limit. See *Test Current Limit* for more details.

For the load with specific operating characteristics as shown in S2 and L2 curves, it is necessary to use a fold-back current limiting device with a higher I_{Short}, or a voltage stabilizing device with a "brick-wall" type current limiting.

9 Application and Implementation

9.2 Application Information (continued)

Test Current Limit

The VS6376 series, VS7500S series and VS75L00S series use the fold-back current limit. When testing this kind of linear voltage regulator with the fold-back current limit, it should be noted that using the electronic load that is very common in the laboratory as the load of the voltage regulator may cause some problems:

1. When the constant current mode (CC) is used for testing, when the load current is higher than the short circuit current (I_{Short}), the device may not be able to start normally from 0V, because the CC mode of the electronic load has similar operating characteristics as the L2 curve described in the fold-back current limit. Moreover, in the CC mode, the internal circuit of the electronic load will try to pull down the output voltage below the ground. A feasible method is to start the device with no load first, and then switch to the required steady state current. A constant resistance (CR) load mode using an electronic load may help, but this may lead to the following other problems.
2. When using the CC mode of the electronic load to test the current limiting behavior, the negative feedback loop with constant internal control current of the electronic load will conflict with the current limiting loop of the device and may cause faults. When the CR mode is used for testing, the complex control loop inside the electronic load that keeps the load resistance constant will interact with the regulator and may oscillate at the output.

The above are some problems that may occur when using electronic load to test the voltage regulator. Using actual resistance as the load is a good solution. When testing the I_{Limit}, the variable resistor can be used as the load. First, set the resistance value of the variable resistor to be large enough so that the output current of the device under test at this time is significantly less than the current at full load, then gradually reduce the load resistance until the output voltage exceeds the specified range, and the load current at this time is the maximum load current. The specified range of output voltage depends on the range that the user thinks can be accepted and the current regulation rate of the voltage regulator. When some voltage regulators are in the fold-back current limit state, the output voltage drops rapidly. For these devices, the load current before the output voltage drops should be considered as the maximum load current. The measurement of short circuit current can be realized by shorting the output or connecting the load resistance of 0Ω.

Compared with the electronic load, the variable resistor may not be so convenient, but the use of variable resistor for current limiting measurement is the only way to ensure that there is no bad interaction between the load and the voltage regulator. If it is necessary to measure the starting characteristics of these devices, a variable resistor must be used.

Recommended Continuous Operating Areas

For the VS6376 series, VS7500S series and VS75L00S series, the working area is limited by dropout voltage, output current, junction temperature and input voltage under continuous working condition. The recommended areas for continuous operation are shown in Figure 9-5:

A. The LDO input and output voltage difference V_{IN} - V_{OUT} must meet the dropout voltage V_{DO} conditions. See *Dropout Voltage* for more details.
B. Rated output current range I_{Rated}.
C. The actual junction temperature T_J of LDO shall not exceed the rated junction temperature. The product of voltage difference and current at both ends of LDO is power consumption, which determines the actual working junction temperature of LDO, so the curve is not linear.

In addition, the working area is limited by the rated $V_{IN\ MIN}$ and $V_{IN\ MAX}$.