VSOA906x Series Operational Amplifiers

1 Introduction

The VSOA906x family of single-, dual-, and quad-channel operational amplifiers represents a new generation of general-purpose, low-power op-amps. Featuring rail-to-rail input and output (RRIO) swings, low quiescent current (typical 780 μA) combined with a wide bandwidth (11 MHz) and very low noise (8 nV/√Hz at 1 kHz) makes this family very attractive for a variety of battery-powered applications that require a good balance between cost and performance, such as audio outputs, motor phase current sensing, photodiode amplification, barcode scanners and white goods. The low input bias current supports these amplifiers to be used in applications with mega-ohm source impedances.

The robust design of the VSOA906x amplifiers provides ease-of-use to the circuit designer: unity-gain stability with capacitive loads of up to 500 pF, integrated RF/EMI rejection filter, no phase reversal in overdrive conditions, and high electro-static discharge (ESD) protection (3kV HBM). The VSOA906x amplifiers are optimized for operation at voltages as low as +1.8 V (±0.9 V) and up to+5.5 V (±2.75 V) at the temperature range of 0 °C to 70 °C, and operation at voltages from +2.0 V (±1.0 V) to +5.5 V (±2.75 V) over the extended temperature range of -40°C to +125°C.

The VSOA9061 (single) is available in SOT23-5L packages. The VSOA9062 (dual) is offered in SOP8, and MSOP8 packages. The quad of VSOA9064 is offered in SOP14 packages.

2 Features

- Wide Bandwidth and High Slew Rate:
  11 MHz and 11.5 V/μs
- Fast Settling: 0.26 μs to 0.1%
- Low Noise: 8 nV/√Hz at 1 kHz
- Low Input Offset Voltage: ±0.5 mV
- Single 1.8 V to 5.5 V Supply Voltage Range at 0°C to 70°C
- Rail-to-Rail Input and Output
- Internal RF/EMI Filter
- Low Supply Current:
  780 μA at 5.5V Supply Per Amplifier
- Extended Temperature Range:
  −40°C to +125°C

3 Applications

- Battery-Powered Instruments:
  Consumer, Industrial, Medical, Notebooks
- Audio Outputs
- Motor Phase Current Sense
- Photodiode Amplification
- Sensor Signal Conditioning:
  Sensor Interfaces, Loop-Powered, Active Filters

4 Available Packages

PART NUMBER	PACKAGE
VSOA9061-M5N	SOT-23-5L
9062-PAN	SOP8
VSOA9062-PDN	MSOP8
VSOA9064-PHN	SOP14

7 Specifications

7.1 Absolute Maximum Ratings

(over operating ambient temperature range, unless otherwise specified)(1)

CHARACTERISTIC		SYMBOL	VALUE	UNIT
Supply voltage[(V+) - (V-)]		V_S	10	V
Signal input pins	Voltage(2)		(V-)-0.5V ~ (V+)+0.5V	V
	Current(2)		±10	mA
Output short-circuit		T_{sc}	Continuous(3)	mA
Maximum junction temperature		$T_{J\ MAX}$	150	°C
Storage temperature		T_{stg}	-65 ~ 150	°C
Soldering temperature & time		T_{solder}	260°C, 10s	-

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum rated conditions for extended periods may affect device reliability.

(2) Input pins are diode-clamped to the power-supply rails. Current limit input signals that can swing more than 0.5V beyond the supply rails to 10mA or less.

(3) Short circuits from outputs to V_S can cause excessive heating and eventual destruction. A heat sink may be required to keep the junction temperature below the absolute maximum. This depends on the power supply voltage and how many amplifiers are shorted. Thermal resistance varies with the amount of PC board metal connected to the package. The specified values are for short traces connected to the leads.

7.2 Recommend Operating Conditions

(over operating ambient temperature range, unless otherwise specified)

PARAMETER		SYMBOL	MIN.	NOM.	MAX.	UNIT
Power supply range	TA = 0 ~ 70℃	V_S	1.8	-	5.5	V
	TA = -40 ~ 125℃		2.0	-	5.5	
Operating ambient temperature		T_A	-40	-	125	°C

7 Specifications

7.3 ESD Ratings

ESD RATINGS		VALUE	UNIT
Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(4)	3000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101(5)	2000	

(4) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(5) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

7.4 Thermal Information

THERMAL METRIC(6)	SYMBOL	SOT-23-5L	SOP8	MSOP8	SOP14	UNIT
Junction-to-ambient thermal resistance	$R_{\Theta JA}$	192.3	125.0	201.6	115.7	°C/W
Reference maximum power dissipation (continuous)	$P_{D\ Ref}$	0.65	1.00	0.62	1.08	W

(6) T_A = 25°C, measured on evaluation board with 1oz. copper traces of minimum pad size, all device outputs were active.

7 Specifications

7.5 Electrical Characteristics

(V_S = (V+) - (V-) = 5.0V, T_A = 25°C, V_{CM} = V_S /2, V_O = V_S /2, and R_L = 10kΩ connected to V_S /2, unless otherwise noted. Boldface limits apply over the specified temperature range, T_A = −40 to +125°C.)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS(7)	MIN.	TYP.	MAX.	UNIT
OFFSET VOLTAGE						
Input offset voltage	V_{OS}	-	-	±0.5	±3	mV
Offset voltage drift	V_{OS} TC	T_A = −40 to +125 °C	-	±1	±3	µV/°C
Power supply rejection ratio	PSRR	V_S = 2.0 to 5.5 V, V_{CM} < (V+) − 2V	95	110	-	dB
		T_A = −40 to +125 ℃	82	-	-	
INPUT VOLTAGE						
Common-mode voltage range	V_{CM}	-	(V-) − 0.1	-	(V+) + 0.1	V
Common-mode rejection ratio	CMRR	V_S = 5.5 V, V_{CM} = −0.1 to 5.6 V	68	84	-	dB
		V_{CM} = 0 to 5.3 V, T_A = −40 to +125℃	65	-	-	
		V_S = 2.0 V, V_{CM} = −0.1 to 2.1 V	65	78	-	
		V_{CM} = 0 to 1.8 V, T_A = −40 to +125℃	62	-	-	
INPUT BIAS CURRENT						
Input bias current	I_B	-	-	1	-	pA
		T_A = +85 °C	-	150	-	
		T_A = +125 °C	-	500	-	
Input offset current	I_{OS}	-	-	1	-	pA
NOISE						
Input voltage noise	E_n	f = 0.1 to 10 Hz	-	3.7	-	μV_{PP}
Input voltage noise density	e_n	f = 1 kHz	-	8	-	nV/√Hz
Input current noise density	I_n	f = 1 kHz	-	5	-	fA/√Hz
INPUT IMPEDANCE						
Input capacitance	C_{IN}	Differential	-	2.0	-	pF
		Common mode	-	3.5	-	
OPEN-LOOP GAIN						
Open-loop voltage gain	A_{VOL}	R_L = 10 kΩ, V_O = 0.05 to 3.5 V	97	105	-	dB
		T_A = −40 to +125 ℃	87	-	-	
		R_L = 600 Ω, V_O = 0.15 to 3.5 V	85	92	-	
		T_A = −40 to +125 ℃	75	-	-	

7 Specifications

7.5 Electrical Characteristics (conitnued)

(V_S = (V+) - (V-) = 5.0V, T_A = 25°C, V_{CM} = V_S /2, V_O = V_S /2, and R_L = 10kΩ connected to V_S /2, unless otherwise noted. Boldface limits apply over the specified temperature range, T_A = −40 to +125°C.)

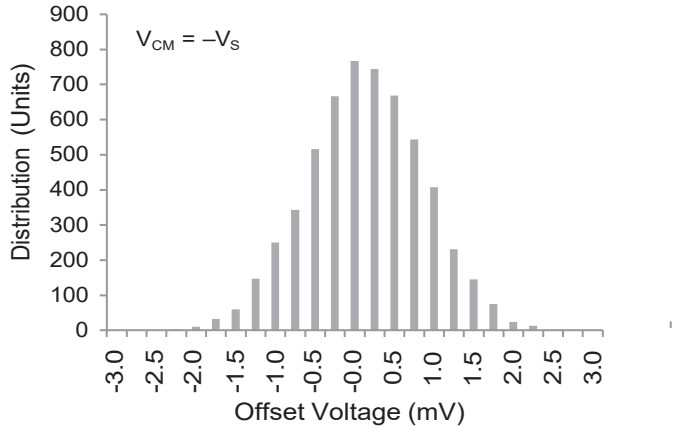
CHARACTERISTIC	SYMBOL	TEST CONDITIONS(7)	MIN.	TYP.	MAX.	UNIT
FREQUENCY RESPONSE						
Gain bandwidth product	GBW	-	-	11	-	MHz
Slew rate	SR	G = +1, C_L = 100 pF, V_O = 1.5 to 3.5 V	-	11.5	-	V/µs
Total harmonic distortion + noise	THD+N	G = +1, f = 1 kHz, V_O = 0.5 V_{RMS}	-	0.0005	-	%
Settling time	t_S	To 0.1%, G = +1, 1V step	-	0.26	-	µs
		To 0.01%, G = +1, 1V step	-	0.34	-	
Overload recovery time	t_{OR}	V_{IN} * Gain > V_S	-	0.3	-	µs
OUTPUT						
High output voltage swing	V_{OH}	R_L = 10 kΩ	(V+) – 12	(V+) – 8	-	mV
		R_L = 600 Ω	(V+) – 180	(V+) – 125	-	
Low output voltage swing	V_{OL}	R_L = 10 kΩ	-	(V-) + 5.5	(V-) + 8	mV
		R_L = 600 Ω	-	(V-) + 88	(V-) + 130	
Short-circuit current	I_{SC}	-	-	+70 / –85	-	mA
POWER SUPPLY						
Quiescent current (per amplifier)	I_Q	V_S = 2.0 V	-	615	740	µA
		V_S = 5.5 V	-	780	940	

7 Specifications

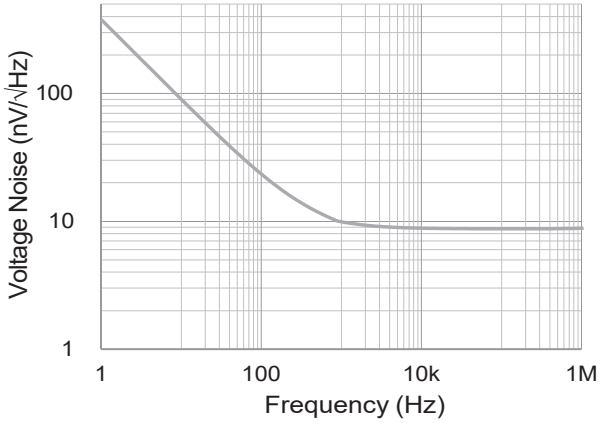
7.6 Typical Characteristics

(V_{CM} = V_S /2, and R_L = 10kΩ connected to V_S /2, T_A = 25°C, unless otherwise specified)

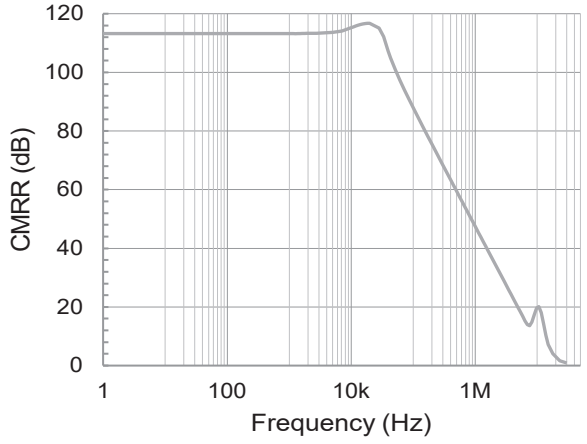
Offset Voltage Production Distribution



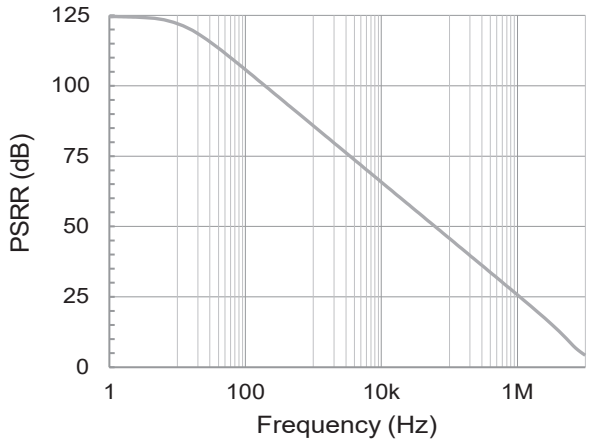
Input Voltage Noise vs. Frequency



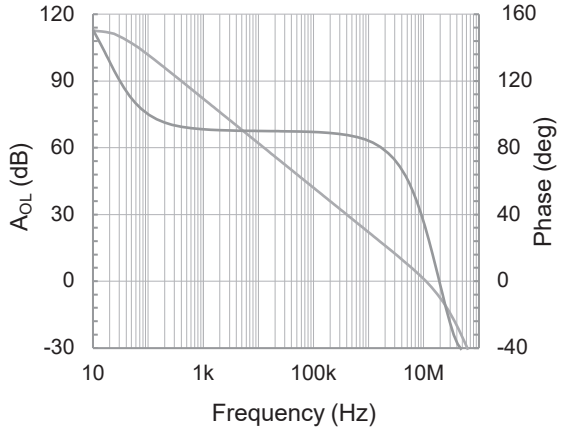
Common-mode Rejection Ratio vs. Frequency



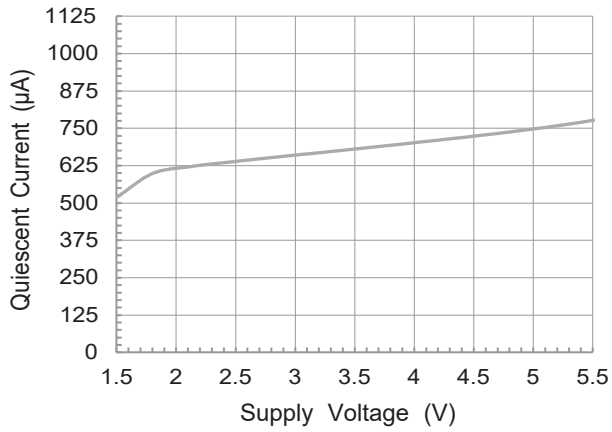
Power Supply Rejection Ratio vs. Frequency



Open-loop Gain and Phase vs. Frequency.



Quiescent Current vs. Supply Voltage.

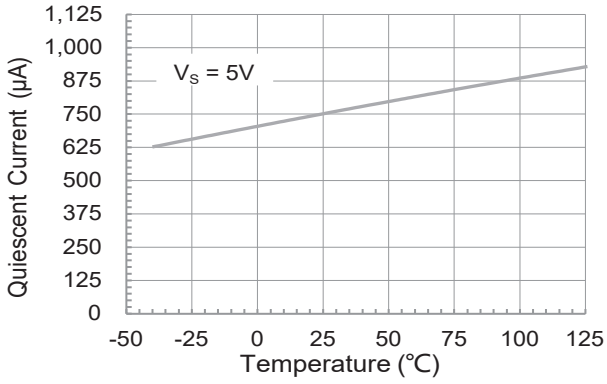


7 Specifications

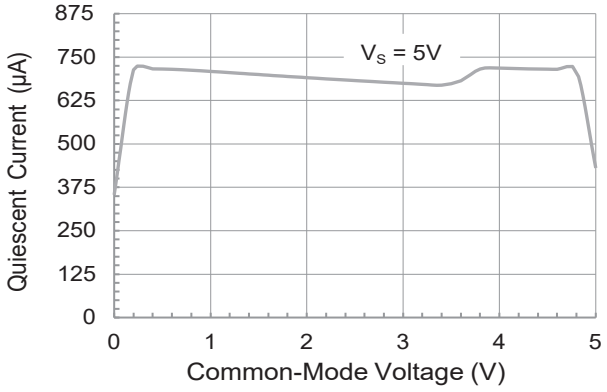
7.6 Typical Characteristics (continued)

(V_{CM} = V_S /2, and R_L = 10kΩ connected to V_S /2, T_A = 25°C, unless otherwise specified)

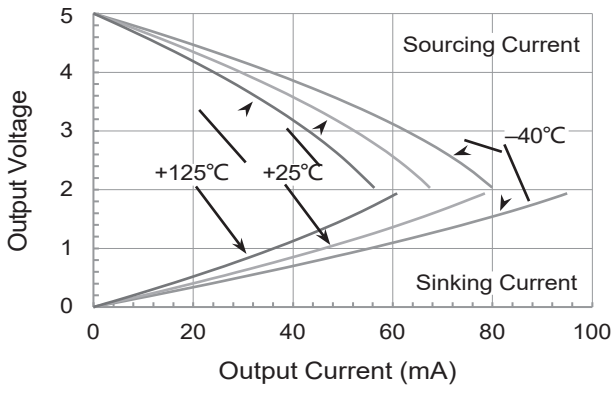
Quiescent Current vs.Temperature



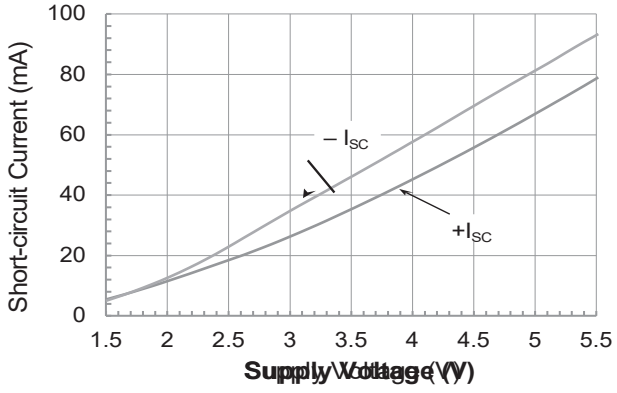
Quiescent Current vs. Input Common-mode Voltage



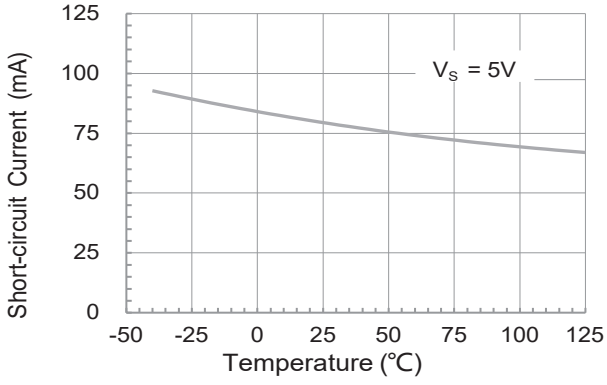
Output Voltage Swing vs. Output Current



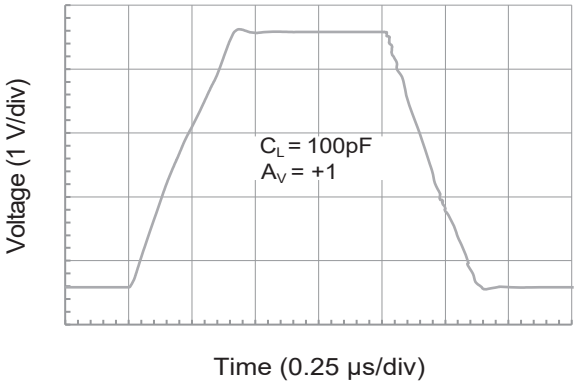
Short-circuit Current vs. Supply Voltage



Short-circuit Current vs. Temperature



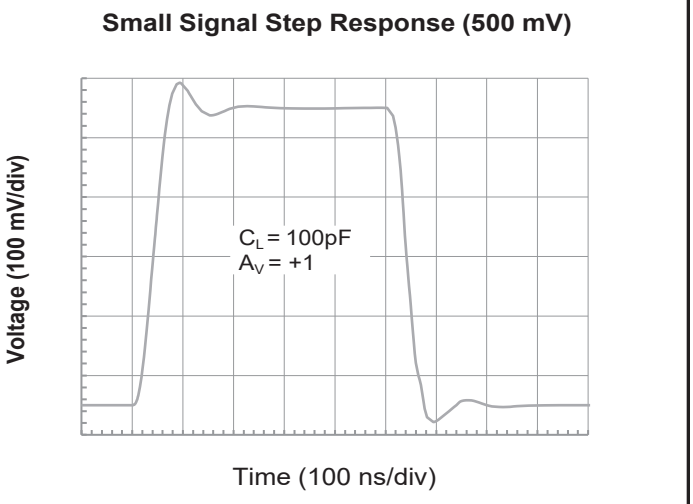
Large Signal Step Response

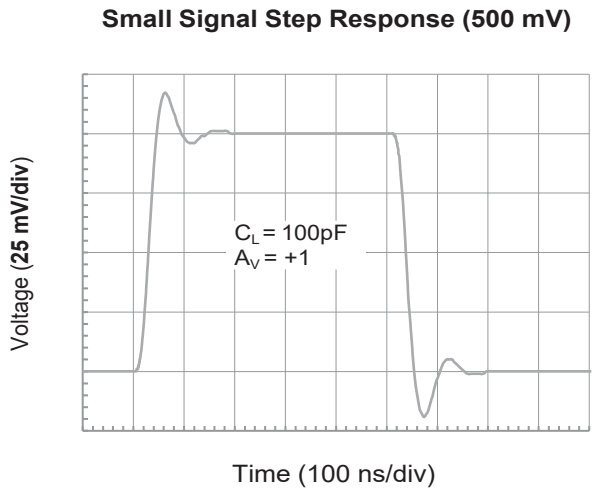


7 Specifications

7.6 Typical Characteristics (continued)

(V_{CM} = V_S /2, and R_L = 10kΩ connected to V_S /2, T_A = 25°C, unless otherwise specified)





8 Detail Description

8.1 Description

The VSOA906x is a family of low-power, rail-to-rail input and output operational amplifiers specifically designed for portable applications. These devices operate from 1.8 V to 5.5 V at the temperature range of 0°C to 70°C, are unity-gain stable, and suitable for a wide range of general-purpose applications. The class AB output stage is capable of driving ≤ 10kΩ loads connected to any point between (V+) and ground. The input common-mode voltage range includes both rails, and allows the VSOA906x family to be used in virtually any single-supply application. Rail-to-rail input and output swing significantly increases dynamic range, especially in low-supply applications, and makes them ideal for driving sampling analog-to-digital converters (ADCs).

8.2 Feature Description

Rail-to-Rail Input

The input common-mode voltage range of the VSOA906x series extends 100mV beyond the negative and positive supply rails. This performance is achieved with a complementary input stage: an N-channel input differential pair in parallel with a P-channel differential pair. The N-channel pair is active for input voltages close to the positive rail, typically (V+) – 1.4 V to the positive supply, whereas the P-channel pair is active for inputs from 100mV below the negative supply to approximately (V+) – 1.4 V. There is a small transition region, typically (V+) – 1.2 V to (V+) – 1 V, in which both pairs are on. This 200mV transition region can vary up to 200mV with process variation. Thus, the transition region (both stages on) can range from (V+) – 1.4 V to (V+) – 1.2 V on the low end, up to (V+) – 1 V to (V+) – 0.8 V on the high end. Within this transition region, PSRR, CMRR, offset voltage, offset drift, and THD can be degraded compared to device operation outside this region.

The typical input bias current of the VSOA906x during normal operation is approximately 1pA. In overdriven conditions, the bias current can increase significantly. The most common cause of an overdriven condition occurs when the operational amplifier is outside of the linear range of operation. When the output of the operational amplifier is driven to one of the supply rails, the feedback loop requirements cannot be satisfied and a differential input voltage develops across the input pins. This differential input voltage results in activation of parasitic diodes inside the front-end input chopping switches that combine with electromagnetic interference (EMI) filter resistors to create the equivalent circuit. Notice that the input bias current remains within specification in the linear region.

Rail-to-Rail Output

Designed as a micro-power, low-noise operational amplifier, the VSOA906x delivers a robust output drive capability. A class AB output stage with common-source transistors is used to achieve full rail-to-rail output swing capability. For resistive loads up to 100kΩ, the output swings typically to within 5mV of either supply rail regardless of the power-supply voltage applied. Different load conditions change the ability of the amplifier to swing close to the rails. For resistive loads up to 600Ω, the output swings typically to within 125mV of the positive supply rail and within 88mV of the negative supply rail.

8 Detail Description

8.2 Feature Description (continued)

Overload Recovery

Overload recovery is defined as the time required for the operational amplifier output to recover from a saturated state to a linear state. The output devices of the operational amplifier enter a saturation region when the output voltage exceeds the rated operating voltage, either because of the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices require time to return back to the linear state. After the charge carriers return back to the linear state, the device begins to slew at the specified slew rate. Thus, the propagation delay in case of an overload condition is the sum of the overload recovery time and the slew time. The overload recovery time for the VSOA906x family is approximately 0.3μs.

EMI Rejection

Circuit performance is often adversely affected by high frequency EMI. When the signal strength is low and transmission lines are long, an op-amp must accurately amplify the input signals. However, all op-amp pins — the non-inverting input, inverting input, positive supply, negative supply, and output pins —are susceptible to EMI signals. These high frequency signals are coupled into an op-amp by various means, such as conduction, near field radiation, or far field radiation. For example, wires and printed circuit board (PCB) traces can act as antennas and pick up high frequency EMI signals. Amplifiers do not amplify EMI or RF signals due to their relatively low bandwidth. However, due to the nonlinearities of the input devices, op-amps can rectify these out of band signals. When these high frequency signals are rectified, they appear as a dc offset at the output.

The VSOA906x op-amps have integrated EMI filters at their input stage. A mathematical method of measuring EMIRR is defined as follows:

$$EMIRR = 20\ log(V_{IN\_PEAK}/\Delta V_{OOS})$$

9 Application and Implementation

9.1 Application Information

The VSOA906x features 11MHz bandwidth and 11.5 V/μs slew rate with only 780μA supply current per amplifier, providing good ac performance at very low power consumption. DC applications are also well served with a low input noise voltage of 8nV/√Hz at 1 kHz, low input bias current, and an input offset voltage of 0.5mV typically. The typical offset voltage drift is 1μV/°C, over the full temperature range the input offset voltage changes only 100μV (0.5mV to 0.6mV).

9.2 Typical Application Circuits

Input EMI Filter and Clamp Circuit

Figure 9-1 shows the input EMI filter and clamp circuit. The VSOA906x op-amps have internal ESD protection diodes (D1, D2, D3, and D4) that are connected between the inputs and each supply rail. These diodes protect the input transistors in the event of electrostatic discharge and are reverse biased during normal operation. This protection scheme allows voltages as high as approximately 500mV beyond the rails to be applied at the input of either terminal without causing permanent damage. These ESD protection current-steering diodes also provide in-circuit, input overdrive protection, as long as the current is limited to 20mA as stated in the Absolute Maximum Ratings.

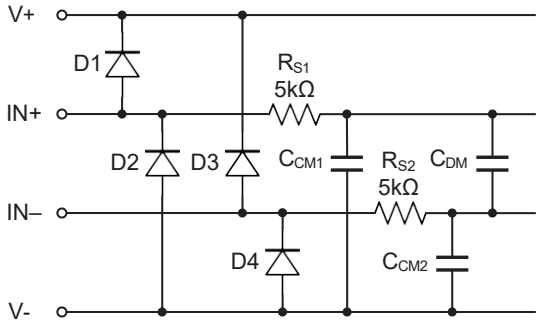


Figure 9-1. Input EMI Filter and Clamp Circuit

Operational amplifiers vary in susceptibility to EMI. If conducted EMI enters the operational amplifier, the dc offset at the amplifier output can shift from its nominal value when EMI is present. This shift is a result of signal rectification associated with the internal semiconductor junctions. Although all operational amplifier pin functions can be affected by EMI, the input pins are likely to be the most susceptible. The EMI filter of the VSOA906x family is composed of two 5kΩ input series resistors (R_{S1} and R_{S2}), two common-mode capacitors (C_{CM1} and C_{CM2}), and a differential capacitor (C_{DM}). These RC networks set the −3 dB low-pass cutoff frequencies at 35MHz for common-mode signals, and at 22MHz for differential signals.

9 Application and Implementation

9.2 Typical Application Circuits (continued)

Capacitive Load and Stability

The VSOA906x family can safely drive capacitive loads of up to 500pF in any configuration. As with most amplifiers, driving larger capacitive loads than specified may cause excessive overshoot and ringing, or even oscillation. A heavy capacitive load reduces the phase margin and causes the amplifier frequency response to peak. Peaking corresponds to over-shooting or ringing in the time domain. Therefore, it is recommended that external compensation be used if the VSOA906x op-amps must drive a load exceeding 500pF. This compensation is particularly important in the unity-gain configuration, which is the worst case for stability.

A quick and easy way to stabilize the op-amp for capacitive load drive is by adding a series resistor, R_{ISO}, between the amplifier output terminal and the load capacitance, as shown in Figure 9-2. R_{ISO} isolates the amplifier output and feedback network from the capacitive load. The bigger the R_{ISO} resistor value, the more stable V_{OUT} will be. Note that this method results in a loss of gain accuracy because R_{ISO} forms a voltage divider with the R_L.

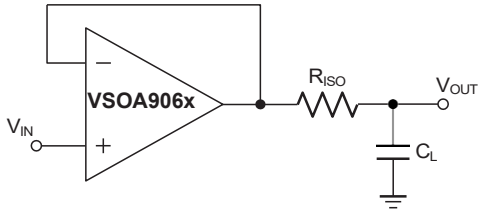


Figure 9-2. Indirectly Driving Heavy Capacitive Load

An improvement circuit is shown in Figure 9-3. It provides DC accuracy as well as AC stability. The RF provides the DC accuracy by connecting the inverting signal with the output.

The CF and RISO serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifier's inverting input, thereby preserving phase margin in the overall feedback loop.

For no-buffer configuration, there are two others ways to increase the phase margin: (a) by increasing the amplifier's gain, or (b) by placing a capacitor in parallel with the feedback resistor to counteract the parasitic capacitance associated with inverting node.

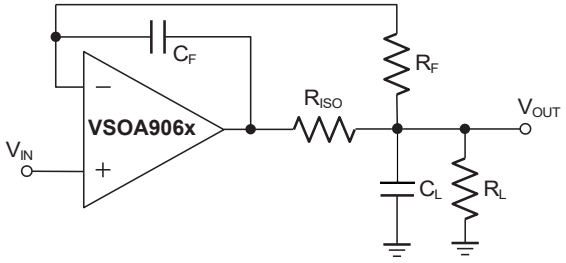


Figure 9-3. Indirectly Driving Heavy Capacitive Load with DC Accuracy

Input-to-Output Coupling

To minimize capacitive coupling, the input and output signal traces should not be parallel. This helps reduce unwanted positive feedback.

9 Application and Implementation

9.2 Typical Application Circuits (continued)

Active Filter

The VSOA906x family is well-suited for active filter applications that require a wide bandwidth, fast slew rate, low-noise, single supply operational amplifier. Figure 9-4 shows a 500kHz, second-order, low-pass filter using the multiple-feedback (MFB) topology. The components have been selected to provide a maximally-flat Butterworth response. Beyond the cut-off frequency, roll-off is –40 dB/dec. The Butterworth response is ideal for applications that require predictable gain characteristics, such as the anti-aliasing filter used in front of an ADC.

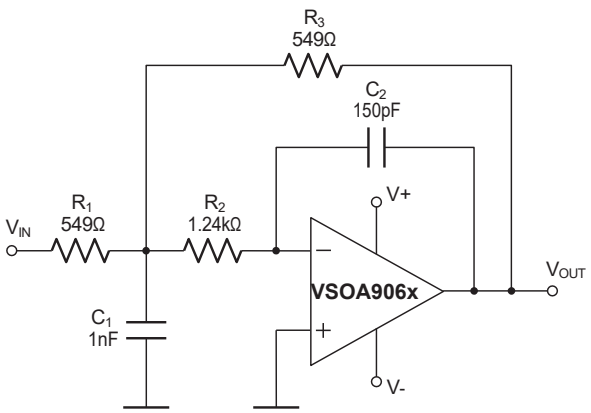


Figure 9-4. Second-Order, Butterworth, 500-kHz Low-Pass Filter

One point to observe when considering the MFB filter is that the output is inverted, relative to the input. If this inversion is not required, or not desired, a non-inverting output can be achieved through one of these options:

1. adding an inverting amplifier;
2. adding an additional second-order MFB stage;
3. using a non-inverting filter topology, such as the Sallen-Key (shown in Figure 9-5).

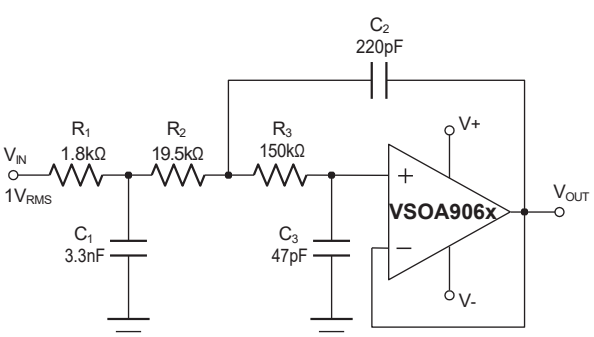


Figure 9-5. Configured as a Three-Pole, 20-kHz, Sallen-Key Filter

Motor Phase Current Sensing

The current sensing amplification shown in Figure 9-6 has a slew rate of $2\pi V_{PP}$ for the output of sine wave signal, and has a slew rate of $2fV_{PP}$ for the output of triangular wave signal. In most of motor control systems, the PWM frequency is at 10 kHz to 20 kHz, and one cycle time is 100 μs for a 10 kHz of PWM frequency. In current shunt monitoring for a motor phase, the phase current is converted to a phase voltage signal for ADC sampling. This sampling voltage signal must be settled before entering the ADC. As the Figure 9-6 shown, the total settling time of a current shunt monitor circuit includes: the rising edge delay time (t_{SR}) due to the op-amp's slew rate, and the measurement settling time (t_{SET}). For a 2-shunt solution of motor phase current sensing, if the minimum duty cycle of the PWM is defined at 5%, and the t_{SR} is required at 20% of a total time window for a phase current monitoring,

9 Application and Implementation

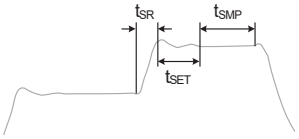
9.2 Typical Application Circuits (continued)

Motor Phase Current Sensing (continued)

in case of a 3.3 V motor control system (3.3 V MCU with 12-bit ADC), the op-amp's slew rate should be more than:

$$\frac{3.3}{(100\mu s \times 5\% \times 20\%)} = 3.3/\mu s$$

At the same time, the op-amp's bandwidth should be much greater than the PWM frequency, like 10 time at least.



t_{SR} – Time delay due to op-amp slew rate
t_{SET} – Measurementsettlingtime
t_{SMP} – Sampling time window

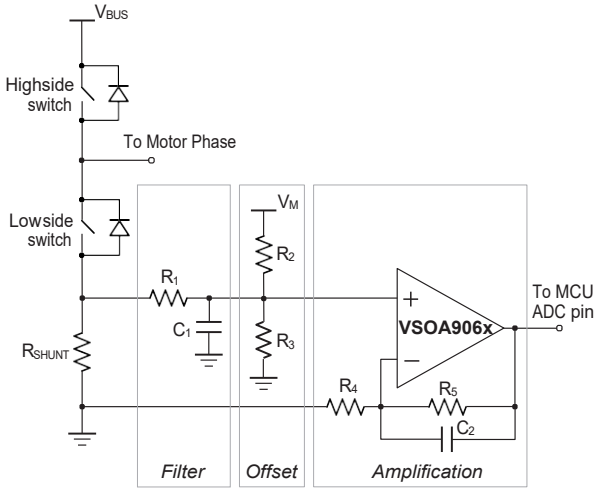


Figure 9-6. Current Shunt Monitor Circuit

Differential Amplifer

The circuit shown in Figure 9-7 performs the difference function. If the resistors ratios are equal $R_4/R_3 = R_2/R_1$, then:

$$V_{OOUT} = (V_p - V_n) \times R_2/R_1 + V_{REF}$$

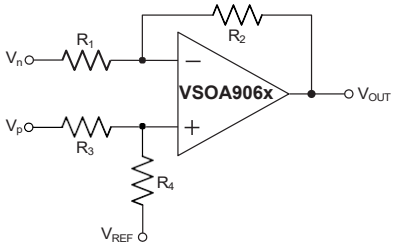


Figure 9-7. Differential Amplifier

9 Application and Implementation

9.4 Layout Guidelines

To achieve the maximum performance of the extremely high input impedance and low offset voltage of the VSOA906x op-amps, care is needed in laying out the circuit board. The PCB surface must remain clean and free of moisture to avoid leakage currents between adjacent traces. Surface coating of the circuit board reduces surface moisture and provides a humidity barrier, reducing parasitic resistance on the board. The use of guard rings around the amplifier inputs further reduces leakage currents. Figure 9-10 shows proper guard ring configuration and the top view of a surface-mount layout. The guard ring does not need to be a specific width, but it should form a continuous loop around both inputs. By setting the guard ring voltage equal to the voltage at the non-inverting input, parasitic capacitance is minimized as well. For further reduction of leakage currents, components can be mounted to the PCB using Teflon standoff insulators.

Other potential sources of offset error are thermoelectric voltages on the circuit board. This voltage, also called Seebeck voltage, occurs at the junction of two dissimilar metals and is proportional to the temperature of the junction. The most common metallic junctions on a circuit board are solder-to-board trace and solder-to-component lead. If the temperature of the PCB at one end of the component is different from the temperature at the other end, the resulting Seebeck voltages are not equal, resulting in a thermal voltage error.

This thermocouple error can be reduced by using dummy components to match the thermoelectric error source. Placing the dummy component as close as possible to its partner ensures both Seebeck voltages are equal, thus canceling the thermocouple error. Maintaining a constant ambient temperature on the circuit board further reduces this error. The use of a ground plane helps distribute heat throughout the board and reduces EMI noise pickup.

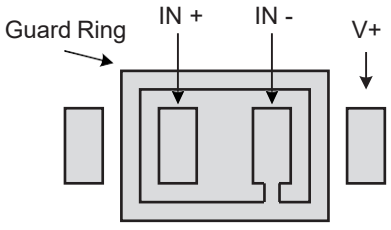


Figure 9-10. Guard Ring