LMV321B, LMV358B and LMV324B CMOS Amplifiers

1 Introduction

The LMV321B/LMV358B/LMV324B family of single, dual, and quad channel operational amplifiers is specifically designed for general-purpose cost-sensitive systems and applications. Featuring rail-to-rail input and output (RRIO) swings, and low quiescent current (typical 85μA) combined with a wide bandwidth (1.2MHz) and low noise (30nV/√Hz at 1kHz) makes this family very attractive for a variety of battery-powered applications that require a good balance between cost and performance, such as audio outputs, consumer electronics, smoke detectors, portable medical devices and white goods. The low input bias current supports these amplifiers to be used in applications with mega-ohm source impedances.

The robust design of the LMV321B/LMV358B/LMV324B family provides ease-of-use to the circuit designer: unity-gain stability with capacitive loads of up to 500pF, integrated RF/EMI rejection filter, no phase reversal in overdrive conditions, and high electro-static discharge (ESD) protection (5kV HBM). The LMV321B/LMV358B/LMV324B amplifiers are optimized for operation at voltages as low as +1.8V (±0.9V) and up to +5.5V (±2.75V), and over the extended temperature range of −40°C to +125°C.

The LMV321B (single) is available in both SOT-23-5L package. The LMV358B (dual) is offered in SOP8, DFNWB2×2-8L and MSOP8 packages. The quad-channel LMV324B is offered in SOP14 and TSSOP14 package.

2 Features

- General Purpose Amplifiers for Cost-Sensitive Systems
- Low Input Offset Voltage:
  ±3.0mV (Max.)
- Low Noise: 30nV/√Hz at 1kHz
- 1.2MHz GBW for Unity-Gain Stable
- Micro-Power:
  85μA Supply Current Per Amplifier
- Single 1.8V to 5.5V Supply Voltage Range
- Rail-to-Rail Input and Output
- Internal RF/EMI Filter
- Extended Temperature Range:
  −40°C to +125°C

3 Applications

- Battery-Powered Instruments:
  Consumer, Industrial, Medical, Notebooks
- Audio Outputs
- Sensor Signal Conditioning:
  Sensor Interfaces, Loop-Powered, Active Filters
- Wireless Sensors:
  Home Security, Remote Sensing, Wireless Metering

4 Available Packages

PART NUMBER	PACKAGE
LMV321B-M5N	SOT-23-5L
LMV358B-PAN	SOP8
LMV358B-PDN	MSOP8
LMV358B-DCN	DFNWB2×2-8L
LMV324B-PHN	SOP14
LMV324B-PIN	TSSOP14

7 Specifications

7.1 Absolute Maximum Ratings

(over operating ambient temperature range, unless otherwise specified)(1)

CHARACTERISTIC		SYMBOL	VALUE	UNIT
Supply voltage[(V+) - (V-)]		V_S	10	V
Signal input pins	Voltage(2)		(V-)-0.5V ~ (V+)+0.5V	V
	Current(2)		±10	mA
Output short-circuit		T_{sc}	Continuous(3)	mA
Maximum junction temperature		$T_{J\ MAX}$	150	°C
Storage temperature		T_{stg}	-65 ~ 150	°C
Soldering temperature & time		T_{solder}	260°C, 10s	-

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum rated conditions for extended periods may affect device reliability.

(2) Input pins are diode-clamped to the power-supply rails. Current limit input signals that can swing more than 0.5V beyond the supply rails to 10mA or less.

(3) Short circuits from outputs to V_S can cause excessive heating and eventual destruction. A heat sink may be required to keep the junction temperature below the absolute maximum. This depends on the power supply voltage and how many amplifiers are shorted. Thermal resistance varies with the amount of PC board metal connected to the package. The specified values are for short traces connected to the leads.

7.2 Recommend Operating Conditions

(over operating ambient temperature range, unless otherwise specified)

PARAMETER		SYMBOL	MIN.	NOM.	MAX.	UNIT
Power supply range	T_A = -40 ~ 125°C	V_S	1.8	-	5.5	V
Operating ambient temperature		T_A	-40	-	125	°C

7 Specifications

7.3 ESD Ratings

ESD RATINGS		VALUE	UNIT
Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(4)	5000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101(5)	2000	
	Machine model (MM), per JESD22-A115C	250	

(4) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(5) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

7.4 Thermal Information

THERMAL METRIC(6)	SYMBOL	LMV321B, LMV358B, LMV324B		UNIT
Junction-to-ambient thermal resistance	$R_{\Theta JA}$	**SOT-23-5L**	**SOP8**	°C/W
		192.3	125.0	
		MSOP8	**SOP14**	
		201.6	115.7	
		DFNWB2×2-8L	**TSSOP14**	
		94.7	119.0	
Reference maximum power dissipation for continuous operation	$P_{D\ Ref}$	**SOT-23-5L**	**SOP8**	W
		0.65	1.00	
		MSOP8	**SOP14**	
		0.62	1.08	
		DFNWB2×2-8L	**TSSOP14**	
		1.32	1.05	

(6) T_A = 25°C, measured on evaluation board with 1oz. copper traces of minimum pad size, all device outputs were active.

7 Specifications

7.5 Electrical Characteristics

(V_S = (V+) - (V-) = 5.0V, T_A = 25°C, V_{CM} = V_S /2, V_O = V_S /2, and R_L = 10kΩ connected to V_S /2, unless otherwise noted. Boldface limits apply over the specified temperature range, T_A = −40 to +125°C.)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
OFFSET VOLTAGE						
Input offset voltage	V_{OS}	-	-	±0.7	±3.0	mV
Offset voltage drift	V_{OS} TC	T_A = −40 to +125°C	-	1.0	3.5	µV/°C
Power supply rejection ratio	PSRR	V_S = 2.0 to 5.5V, V_{CM} < (V+)−2V	80	110	-	dB
		T_A = −40 to +125°C	75	-	-	
INPUT VOLTAGE						
Common-mode voltage range	V_{CM}	-	(V-)−0.1	-	(V+)+0.1	V
Common-mode rejection ratio	CMRR	V_S = 5.5V, V_{CM} = −0.1 to 5.6V	70	83	-	dB
		V_{CM} = 0 to 5.3V, T_A = −40 to +125°C	65	-	-	
		V_S = 2.0V, V_{CM} = −0.1 to 2.1V	65	77	-	
		V_{CM} = 0 to 1.8V, T_A = −40 to +125°C	60	-	-	
INPUT BIAS CURRENT						
Input bias current	I_B	-	-	5	50	pA
		T_A = +85°C	-	-	200	
		T_A = +125°C	-	-	2000	
Input offset current	I_{OS}	-	-	10	50	pA
NOISE						
Input voltage noise	E_n	f = 0.1 to 10Hz	-	6	-	μV_{PP}
Input voltage noise density	e_n	f = 10kHz	-	27	-	nV/√Hz
		f = 1kHz	-	30	-	
Input current noise density	I_n	f = 1kHz	-	5	-	fA/√Hz
INPUT IMPEDANCE						
Input capacitance	C_{IN}	Differential	-	2.0	-	pF
		Common mode	-	3.5	-	
OPEN-LOOP GAIN						
Open-loop voltage gain	A_{VOL}	R_L = 50kΩ, V_O = 0.05 to 3.5V	90	105	-	dB
		T_A = −40 to +125°C	85	-	-	
		R_L = 2kΩ, V_O = 0.15 to 3.5V	85	100	-	
		T_A = −40 to +125°C	80	-	-	

7 Specifications

7.5 Electrical Characteristics (conitnued)

(V_S = (V+) - (V-) = 5.0V, T_A = 25°C, V_{CM} = V_S /2, V_O = V_S /2, and R_L = 10kΩ connected to V_S /2, unless otherwise noted. Boldface limits apply over the specified temperature range, T_A = −40 to +125°C.)

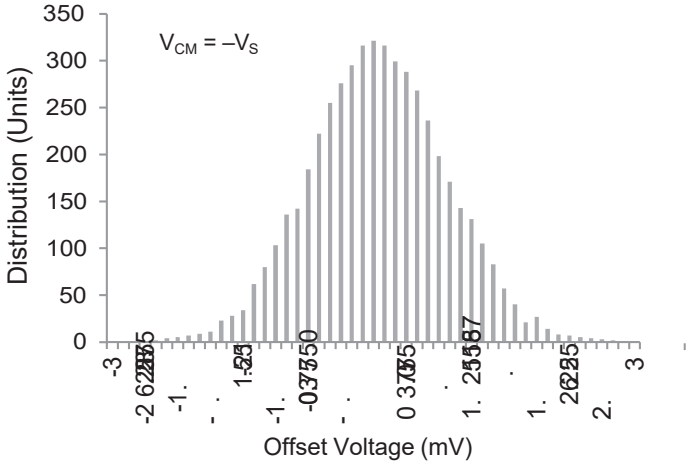
CHARACTERISTIC	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
FREQUENCY RESPONSE						
Gain bandwidth product	GBW	-	-	1.2	-	MHz
Slew rate	SR	G = +1, C_L = 100pF, V_O = 1.5 to 3.5V	-	1	-	V/μs
Total harmonic distortion + noise	THD+N	G = +1, f = 1kHz, V_O = $1V_{RMS}$	-	0.003	-	%
Settling time	t_S	To 0.1%, G = +1, 1V step	-	1.5	-	μs
		To 0.01%, G = +1, 1V step	-	1.8	-	
Overload recovery time	t_{OR}	V_{IN} × Gain > V_S	-	2.5	-	μs
OUTPUT						
High output voltage swing	V_{OH}	R_L = 50kΩ	(V+)–6	(V+)–3	-	mV
		R_L = 2kΩ	(V+)–100	(V+)–65	-	
Low output voltage swing	V_{OL}	R_L = 50kΩ	-	(V-)+2	(V-)+4	mV
		R_L = 2kΩ	-	(V-)+42	(V-)+65	
Short-circuit current	I_{SC}	Source current through 10Ω	-	40	-	mA
		Sink current through 10Ω	-	50	-	
POWER SUPPLY						
Quiescent current (per amplifier)	I_Q	-	-	85	120	μA
		T_A = −40 to +125°C	-	-	150	

7 Specifications

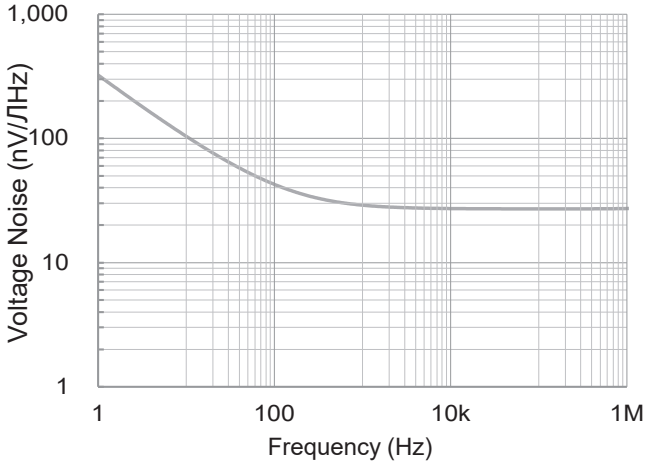
7.6 Typical Characteristics

(V_{CM} = V_S /2, and R_L = 10kΩ connected to V_S /2, T_A = 25°C, unless otherwise specified)

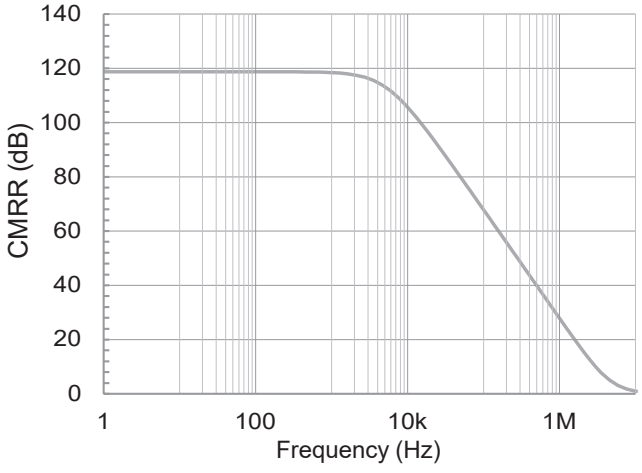
Offset Voltage Production Distribution



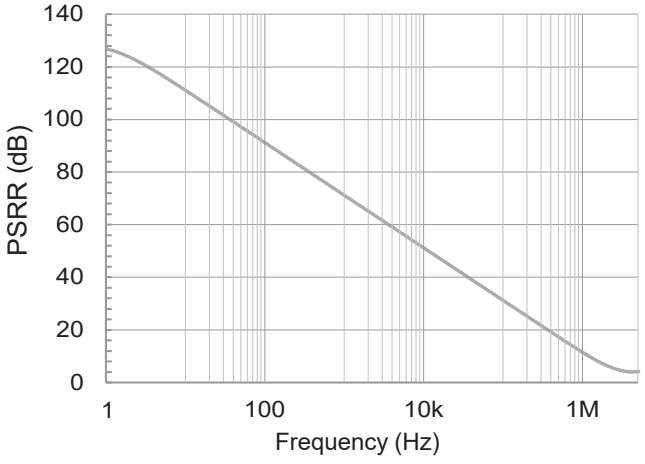
Input Voltage Noise Spectral Density vs. Frequency



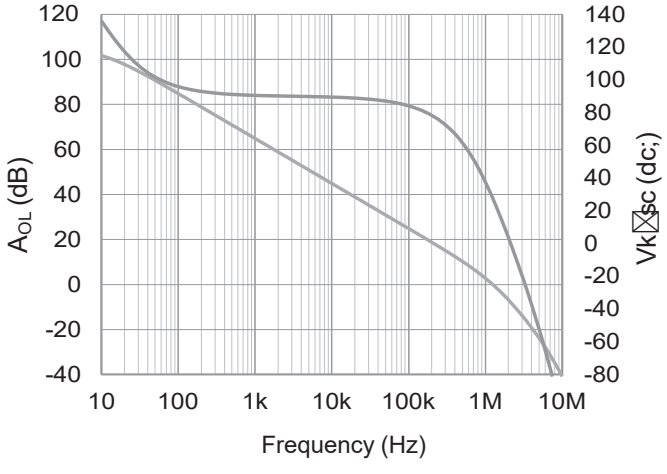
Common-mode Rejection Ratio vs. Frequency



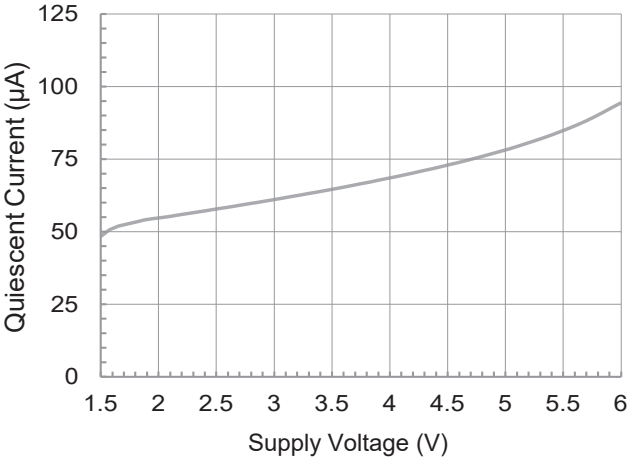
Power Supply Rejection Ratio vs. Frequency



Open-loop Gain and Phase vs. Frequency



Quiescent Current vs. Supply Voltage

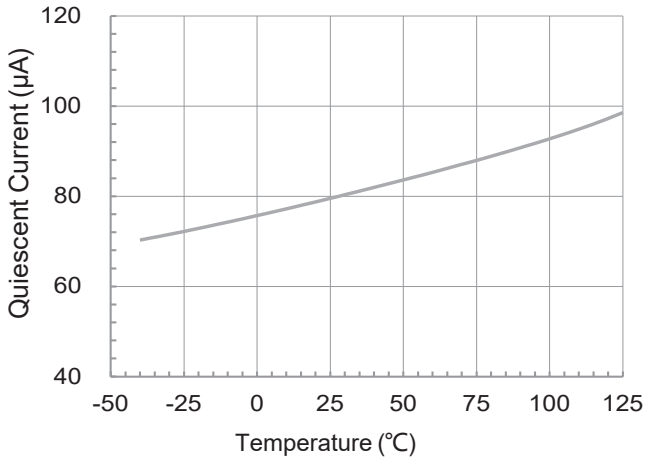


7 Specifications

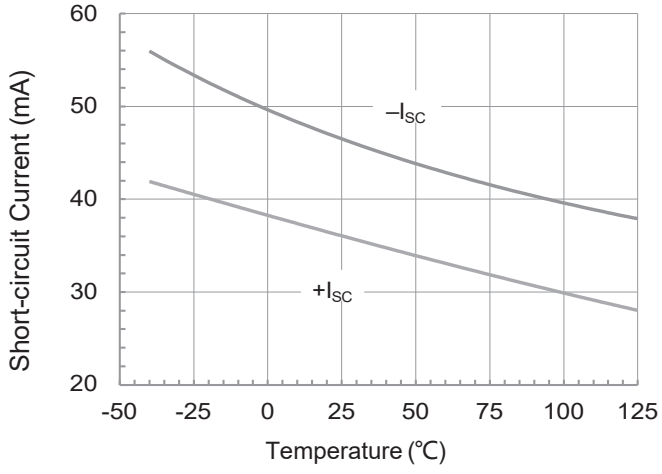
7.6 Typical Characteristics (continued)

(V_{CM} = V_S /2, and R_L = 10kΩ connected to V_S /2, T_A = 25°C, unless otherwise specified)

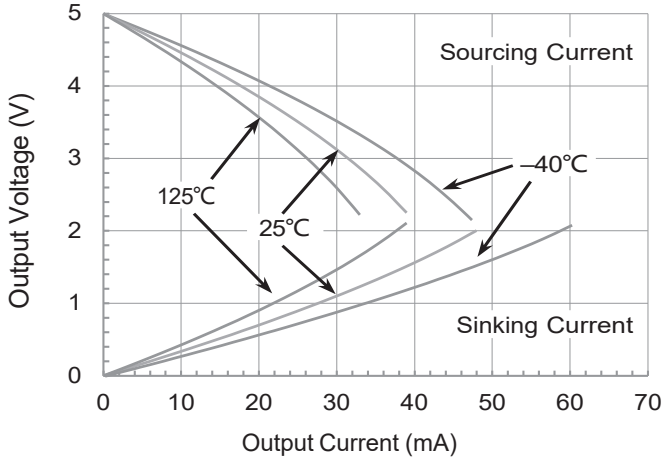
Quiescent Current vs.Temperature



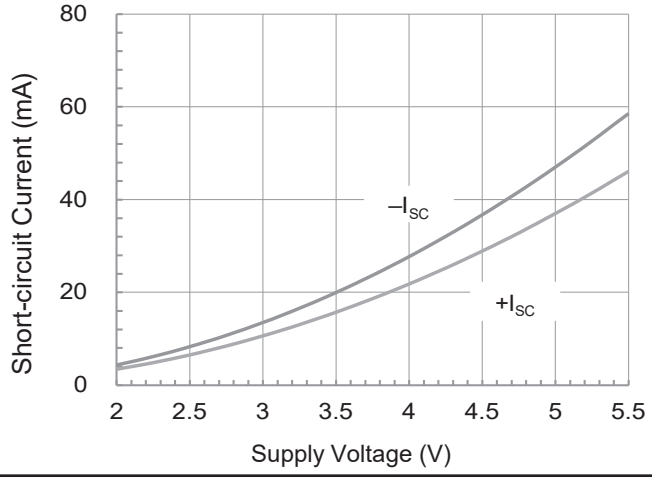
Short-circuit Current vs. Temperature



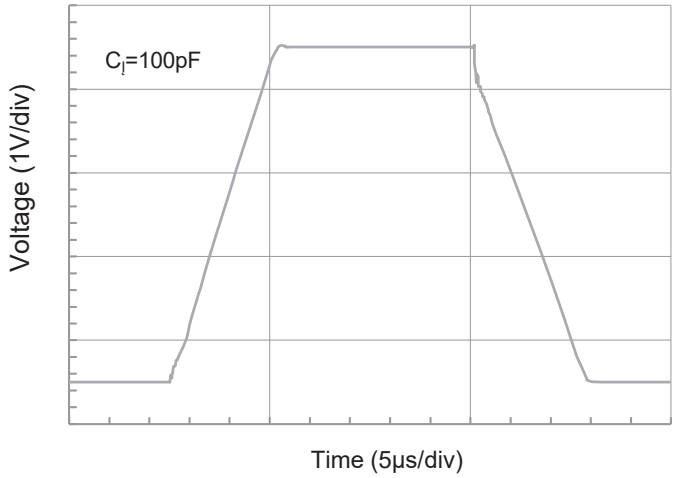
Output Voltage Swing vs. Output Current



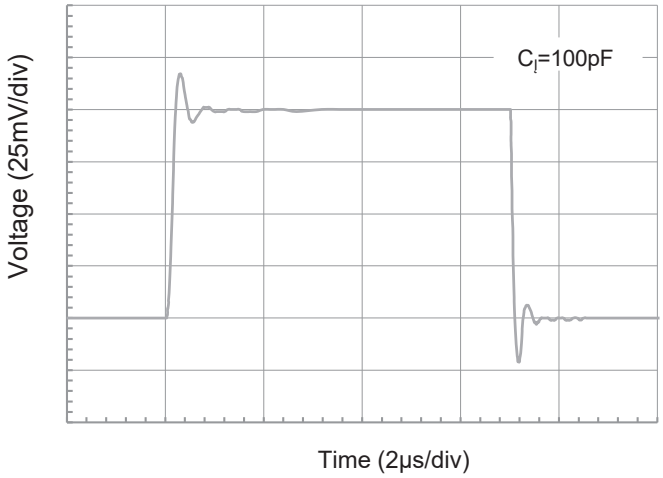
Short-circuit Current vs. Supply Voltage



Large Signal Step Response



Small Signal Step Response



8 Detail Description

8.1 Description

The LMV321B/LMV358B/LMV324B is a family of low-power, rail-to-rail input and output operational amplifiers specifically designed for portable applications. These devices operate from 1.8V to 5.5V, are unity-gain stable, and suitable for a wide range of general-purpose applications. The class AB output stage is capable of driving ≤10kΩ loads connected to anypoint between V+ and ground. The input common-mode voltage range includes both rails, and allows the LMV321B/LMV358B/LMV324B family to be used in virtually any single-supply application. Rail-to-rail input and output swing significantly increases dynamic range, especially in low-supply applications, and makes them ideal for driving sampling analog-to-digital converters (ADCs).

8.2 Feature Description

Rail-to-Rail Input

The input common-mode voltage range of the LMV321B/LMV358B/LMV324B series extends 100mV beyond the negative and positive supply rails. This performance is achieved with a complementary input stage: an N-channel input differential pair in parallel with a P-channel differential pair. The N-channel pair is active for input voltages close to the positive rail, typically (V+)–1.4V to the positive supply, whereas the P-channel pair is active for inputs from 100mV below the negative supply to approximately (V+)–1.4V. There is a small transition region, typically (V+)–1.2V to (V+)–1V, in which both pairs are on. This 200mV transition region can vary up to 200mV with process variation. Thus, the transition region (both stages on) can range from (V+)–1.4V to (V+)–1.2V on the low end, up to (V+)–1V to (V+)–0.8V on the high end. Within this transition region, PSRR, CMRR, offset voltage, offset drift, and THD can be degraded compared to device operation outside this region.

The typical input bias current of the LMV321B/LMV358B/LMV324B during normal operation is approximately 5pA. In overdriven conditions, the bias current can increase significantly. The most common cause of an overdriven condition occurs when the operational amplifier is outside of the linear range of operation. When the output of the operational amplifier is driven to one of the supply rails, the feedback loop requirements cannot be satisfied and a differential input voltage develops across the input pins. This differential input voltage results in activation of parasitic diodes inside the front-end input chopping switches that combine with electromagnetic interference (EMI) filter resistors to create the equivalent circuit. Notice that the input bias current remains within specification in the linear region.

Rail-to-Rail Output

Designed as a micro-power, low-noise operational amplifier, the LMV321B/LMV358B/LMV324B delivers a robust output drive capability. A class AB output stage with common-source transistors is used to achieve full rail-to-rail output swing capability. For resistive loads up to 50kΩ, the output swings typically to within 3mV of either supply rail regardless of the power-supply voltage applied. Different load conditions change the ability of the amplifier to swing close to the rails. For resistive loads up to 2kΩ, the output swings typically to within 65mV of the positive supply rail and within 42mV of the negative supply rail.

8 Detail Description

8.2 Feature Description (continued)

Overload Recovery

Overload recovery is defined as the time required for the operational amplifier output to recover from a saturated state to a linear state. The output devices of the operational amplifier enter a saturation region when the output voltage exceeds the rated operating voltage, either because of the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices require time to return back to the linear state. After the charge carriers return back to the linear state, the device begins to slew at the specified slew rate. Thus, the propagation delay in case of an overload condition is the sum of the overload recovery time and the slew time. The overload recovery time for the LMV321B, LMV358B and LMV324B family is approximately 2.5μs.

EMI Rejection

Circuit performance is often adversely affected by high frequency EMI. When the signal strength is low and transmission lines are long, an op-amp must accurately amplify the input signals. However, all op-amp pins — the non-inverting input, inverting input, positive supply, negative supply, and output pins —are susceptible to EMI signals. These high frequency signals are coupled into an op-amp by various means, such as conduction, near field radiation, or far field radiation. For example, wires and printed circuit board (PCB) traces can act as antennas and pick up high frequency EMI signals. Amplifiers do not amplify EMI or RF signals due to their relatively low bandwidth. However, due to the nonlinearities of the input devices, op-amps can rectify these out of band signals. When these high frequency signals are rectified, they appear as a dc offset at the output.

The LMV321B, LMV358B and LMV324B op-amps have integrated EMI filters at their input stage. A mathematical method of measuring EMIRR is defined as follows:

$$EMIRR = 20\,log(V_{IN\_PEAK}/\Delta V_{OS})$$

9 Application and Implementation

9.1 Application Information

The LMV321B/LMV358B/LMV324B features 1.2MHz bandwidth and 1V/μs slew rate with only 85μA supply current per amplifier, providing good ac performance at very low power consumption. DC applications are also well served with a low input noise voltage of 30nV/√Hz at 1kHz, low input bias current, and an input offset voltage of ±3.0mV maximum. The typical offset voltage drift is 1μV/°C, over the full temperature range the input offset voltage changes only 100μV(0.7mV to 0.8mV).

9.2 Typical Application Circuits

Input EMI Filter and Clamp Circuit

Figure 9-1 shows the input EMI filter and clamp circuit. The LMV321B/LMV358B/LMV324B op-amps have internal ESD protection diodes (D1, D2, D3, and D4) that are connected between the inputs and each supply rail. These diodes protect the input transistors in the event of electrostatic discharge and are reverse biased during normal operation. This protection scheme allows voltages as high as approximately 500mV beyond the rails to be applied at the input of either terminal without causing permanent damage. These ESD protection current-steering diodes also provide in-circuit, input overdrive protection, as long as the current is limited to 20mA as stated in the Absolute Maximum Ratings.

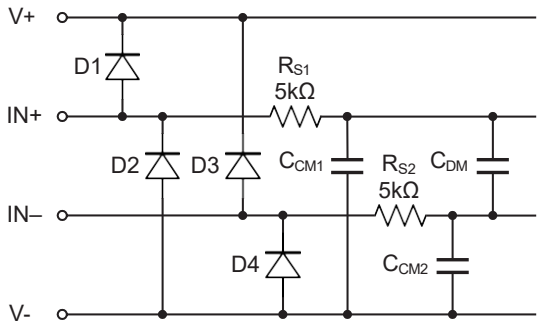


Figure 9-1. Input EMI Filter and Clamp Circuit

Operational amplifiers vary in susceptibility to EMI. If conducted EMI enters the operational amplifier, the dc offset at the amplifier output can shift from its nominal value when EMI is present. This shift is a result of signal rectification associated with the internal semiconductor junctions. Although all operational amplifier pin functions can be affected by EMI, the input pins are likely to be the most susceptible. The EMI filter of the LMV321B/LMV358B/LMV324B family is composed of two 5kΩ input series resistors (R_{S1} and R_{S2}), two common-mode capacitors (C_{CM1} and C_{CM2}), and a differential capacitor (C_{DM}). These RC networks set the −3dB low-pass cutoff frequencies at 35MHz for common-mode signals, and at 22MHz for differential signals.

9 Application and Implementation

9.2 Typical Application Circuits (continued)

Capacitive Load and Stability

The LMV321B/LMV358B/LMV324B family can safely drive capacitive loads of up to 500pF in any configuration. As with most amplifiers, driving larger capacitive loads than specified may cause excessive overshoot and ringing, or even oscillation. A heavy capacitive load reduces the phase margin and causes the amplifier frequency response to peak. Peaking corresponds to over-shooting or ringing in the time domain. Therefore, it is recommended that external compensation be used if the LMV321B/LMV358B/LMV324B op-amps must drive a load exceeding 500pF. This compensation is particularly important in the unity-gain configuration, which is the worst case for stability.

A quick and easy way to stabilize the op-amp for capacitive load drive is by adding a series resistor, R_{ISO}, between the amplifier output terminal and the load capacitance, as shown in Figure 9-2. R_{ISO} isolates the amplifier output and feedback network from the capacitive load. The bigger the R_{ISO} resistor value, the more stable V_{OUT} will be. Note that this method results in a loss of gain accuracy because R_{ISO} forms a voltage divider with the R_L.

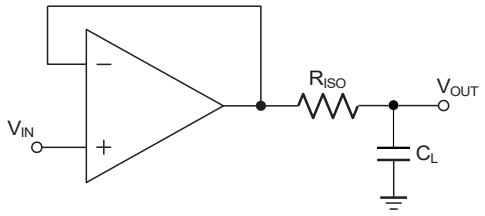


Figure 9-2. Indirectly Driving Heavy Capacitive Load

An improvement circuit is shown in Figure 9-3. It provides DC accuracy as well as AC stability. The R_F provides the DC accuracy by connecting the inverting signal with the output.

The C_F and R_{ISO} serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifier's inverting input, thereby preserving phase margin in the overall feedback loop.

For no-buffer configuration, there are two others ways to increase the phase margin: (a) by increasing the amplifier's gain, or (b) by placing a capacitor in parallel with the feedback resistor to counteract the parasitic capacitance associated with inverting node.

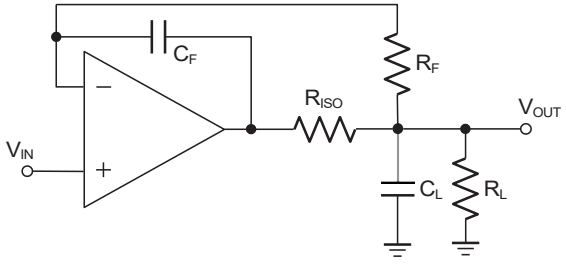


Figure 9-3. Indirectly Driving Heavy Capacitive Load with DC Accuracy

Input-to-Output Coupling

To minimize capacitive coupling, the input and output signal traces should not be parallel. This helps reduce unwanted positive feedback.